

Compal Confidential

Model Name : JE50-HR/SJV50-HR  
Compal Project Name : P5WE0/P5WS0  
File Name : LA-6901P

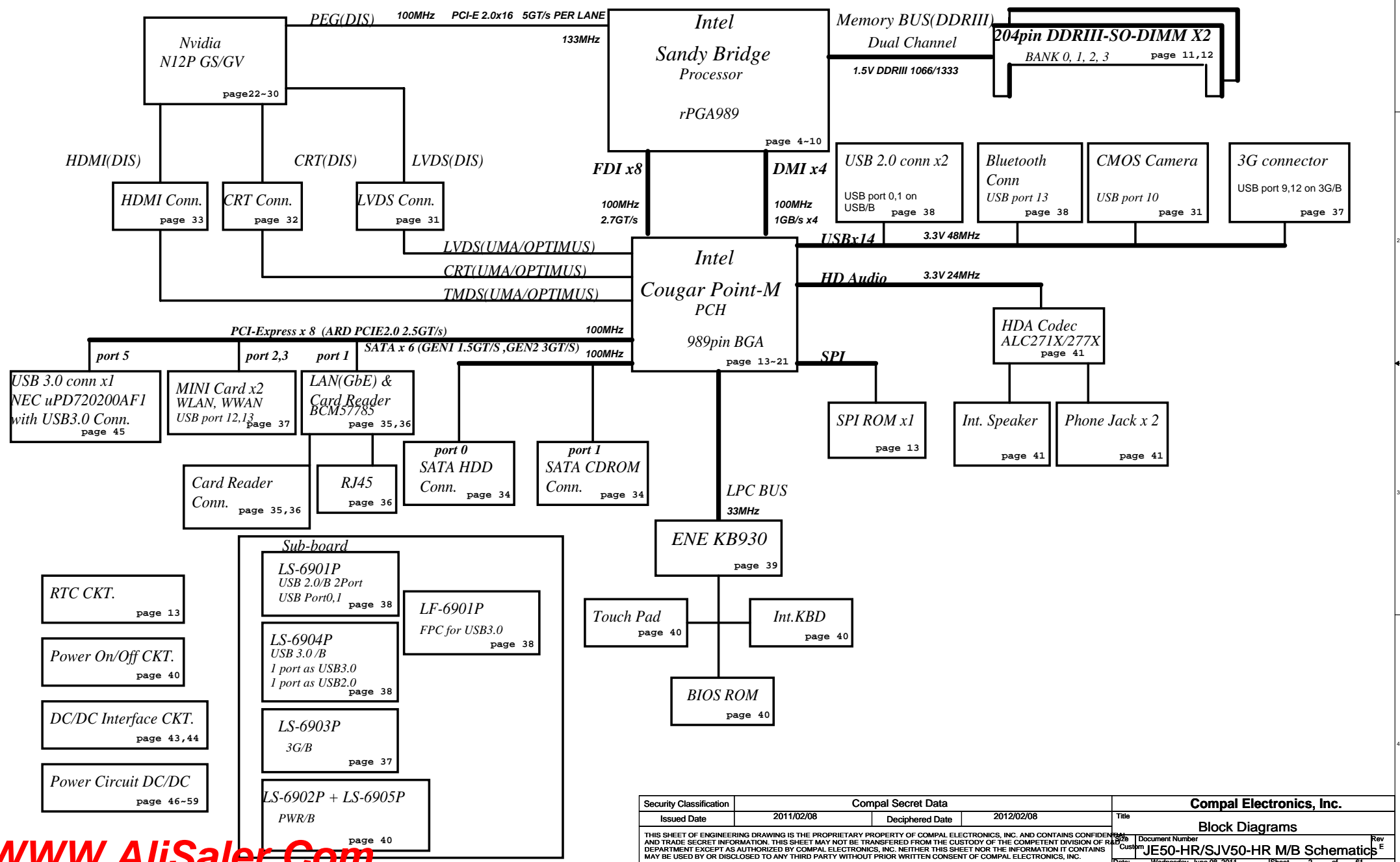
Compal Confidential

JE50-HR/SJV50-HR(P5WE0/P5WS0) M/B Schematics Document  
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH  
Nvidia N12P GS/GV

2011-02-08

REV: 2.0

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

## PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

## 3G & BT & USB30 & USB20 Config

3G SKU: 3G@ USB30 SKU: USB30@ OPTMIUS SKU:OPT@  
 BT SKU: BT@ USB20 SKU: USB20@ Non-OPTMIUS SKU:NOPT@  
 LAN Chip A0 version: A0@ N12P-GS:GS@  
 LAN chip B0 Version: B0@ N12P-GV:GV@

## BOM Config

UMA Only: BT@3G@/USB30@/UMA@/UMAO@/NOPT@/A0@  
 OPTIMUS (N12P-GS): BT@3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GS@  
 DIS Only (N12P-GS): BT@3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GS@  
 OPTIMUS (N12P-GV): BT@3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GV@  
 DIS Only (N12P-GV): BT@3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GV@  
 VRAM P/N : 64\*16  
 Samsung : SA000035700  
 Hynix : SA000032400/SA0000324C0  
 128\*16  
 Samsung : SA00003MQ40  
 Hynix : SA00003VS00

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT  
 EVT2  
 DVT  
 PVT  
 Pre-MP

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

## BTO Option Table

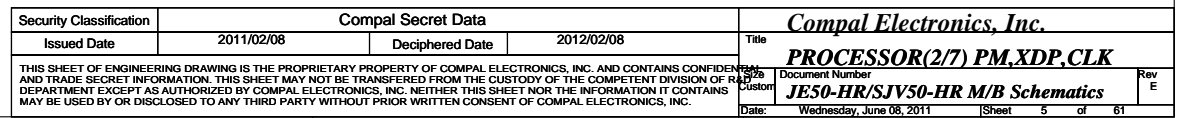
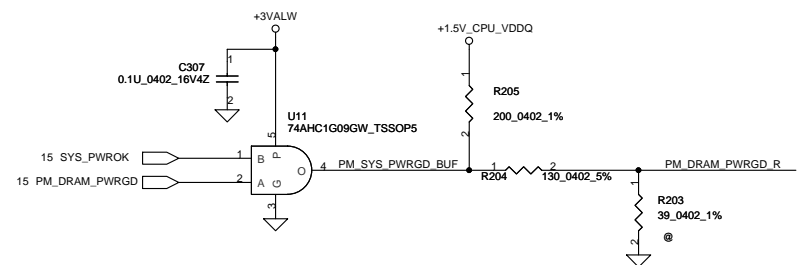
BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@
N12P-GS	GS@
N12P-GV	GV@

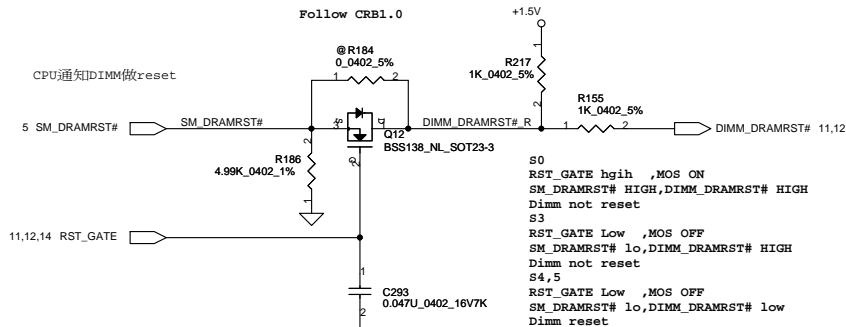
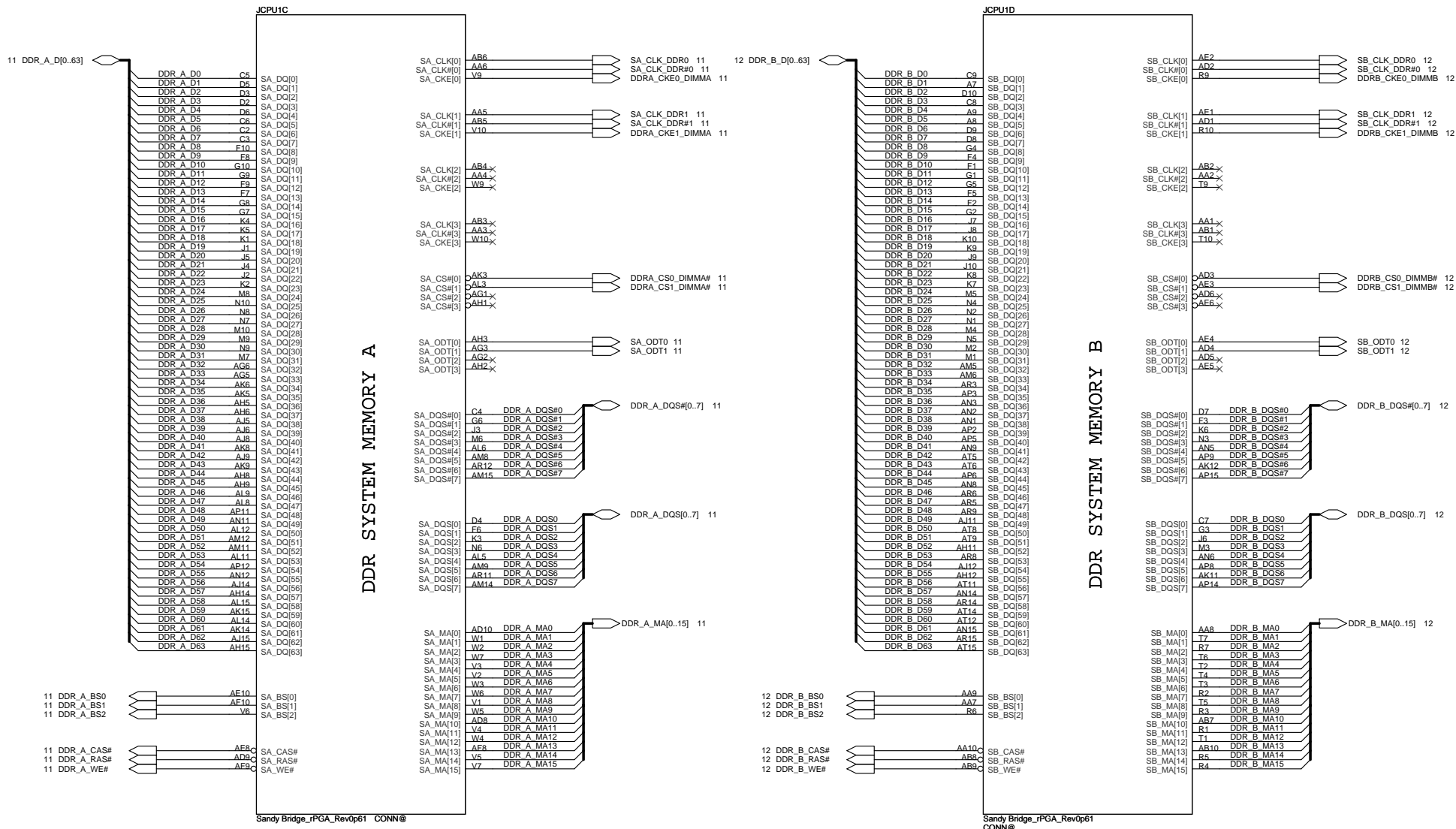
## USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
		2	USB3.0 colay USB2.0 Conn.
	UHCI1	3	USB/B Colay USB3.0
		4	
	UHCI2	5	
EHCI2	UHCI3	6	
		7	
		8	Mini Card 1(WLAN)
	UHCI4	9	3G/B(WWAN)
		10	Camera
	UHCI5	11	Mini Card 2(Reserved)
	UHCI6	12	3G/B(SIM Card)
		13	BlueTooth

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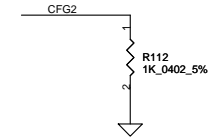




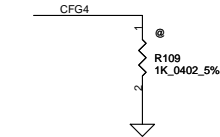


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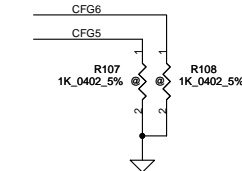
## CFG Straps for Processor



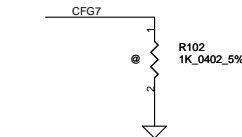
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



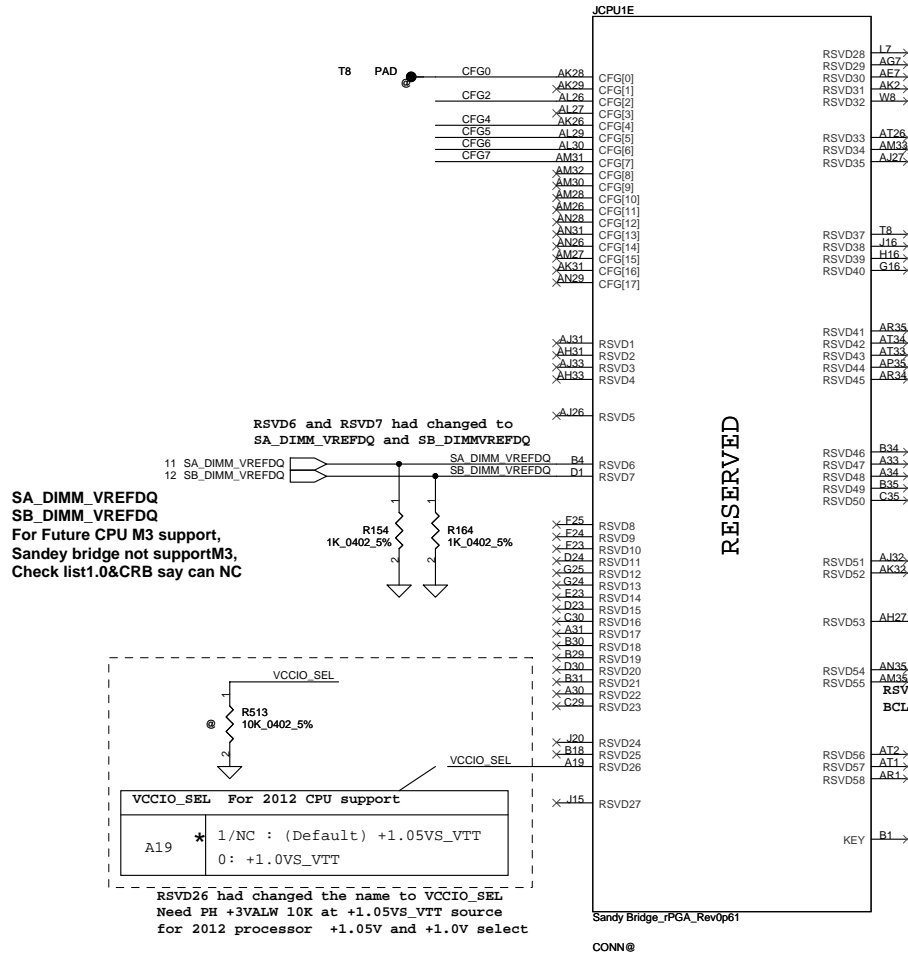
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



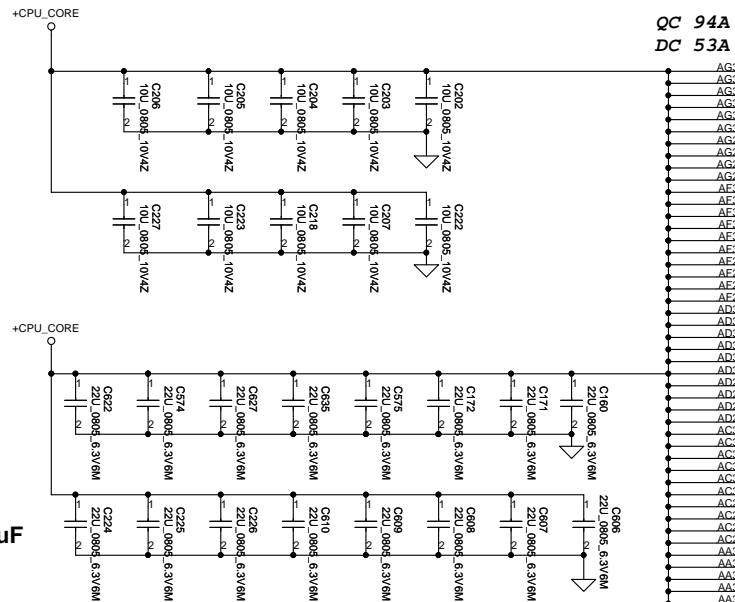
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



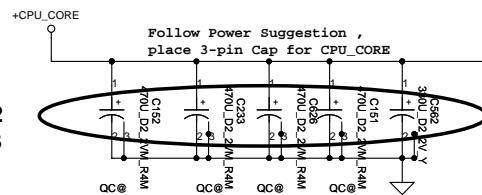
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



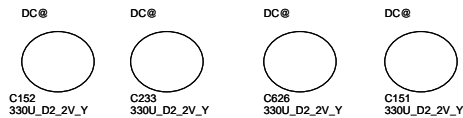
## POWER



**INTEL Recommend  
4\*470uF,16\*22uF and 10\*10uF  
from PDDG 1.0**



PAW00  
use 470uF\*2  
330uF\*3

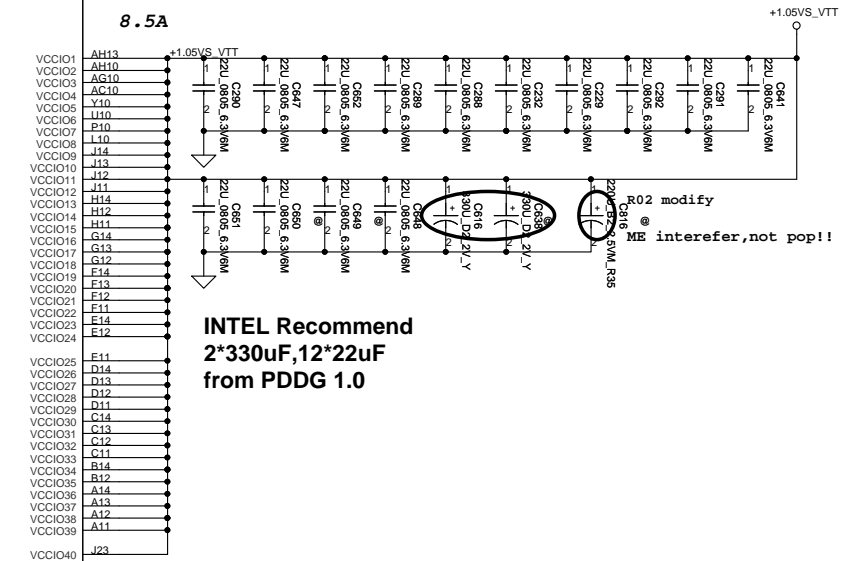


Follow Power Suggestion ,  
place 3-pin Cap for CPU\_C

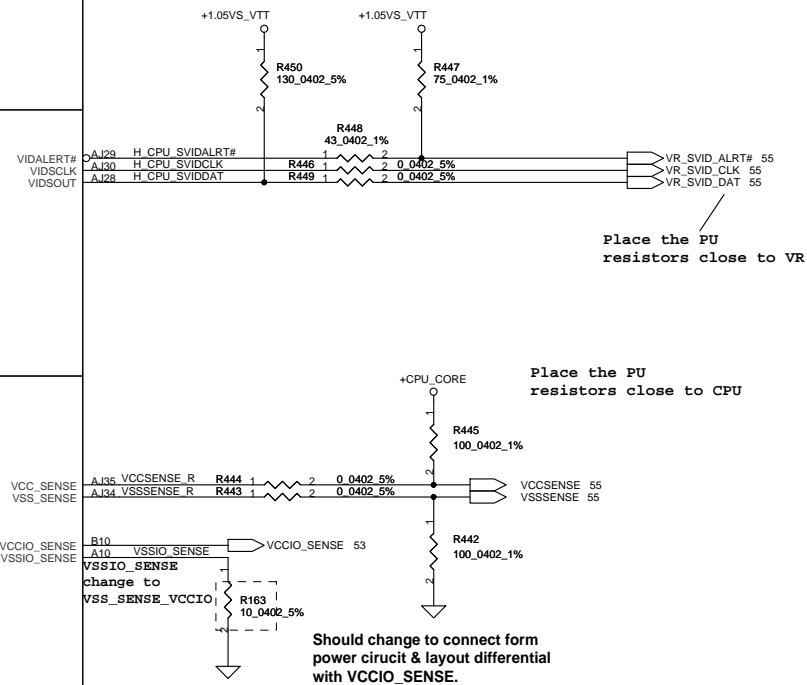
CORE SUPPLY

SVID

SENSE LINES



**INTEL Recommend  
2\*330uF,12\*22uF  
from PDDG 1.0**



Place the PU  
resistors close to VR

Place the PU  
resistors close to CPU

Should change to connect form power cirucit & layout differential with VCCIO\_SENSE.

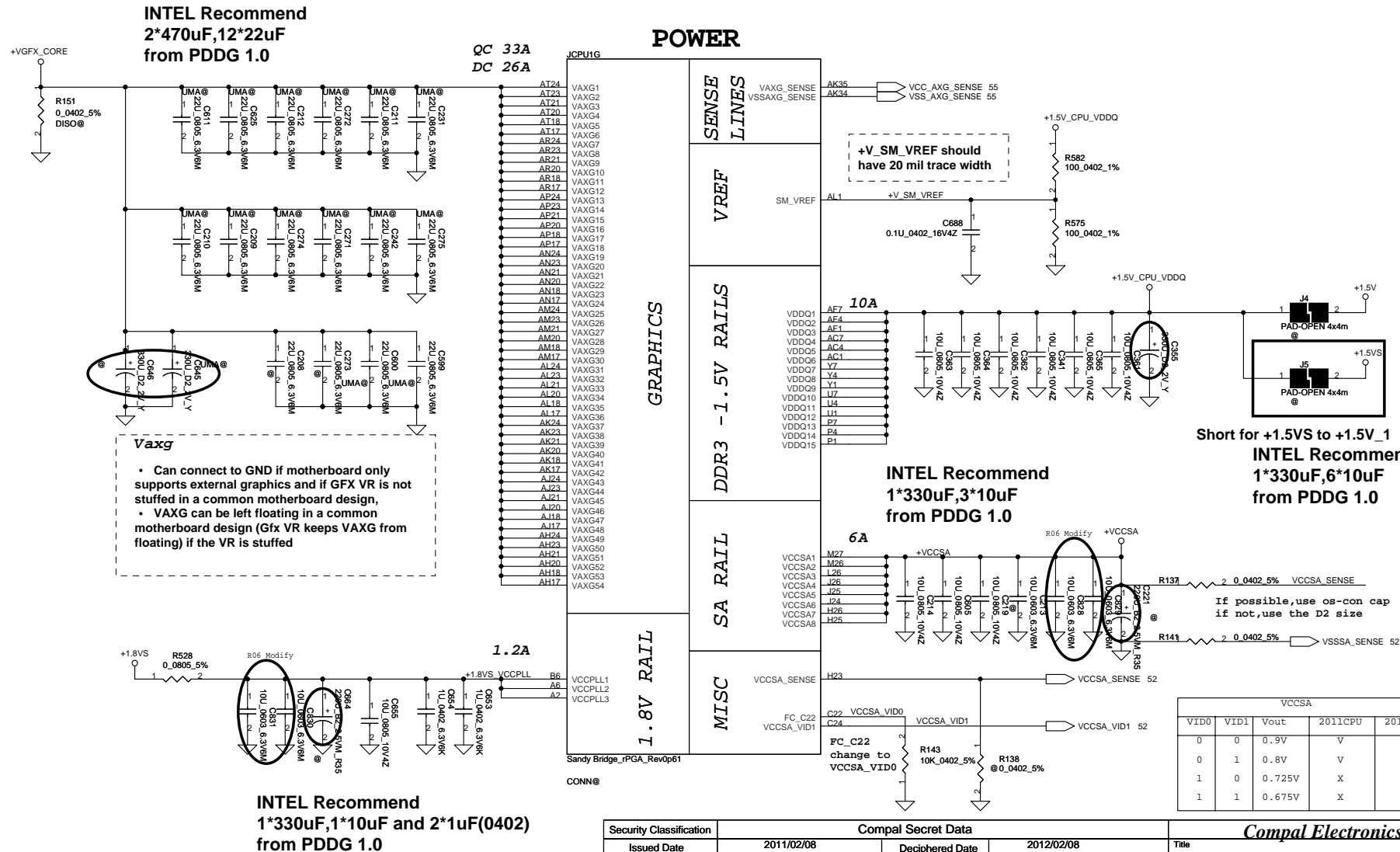
Sandy Bridge rPGA Rev0p61

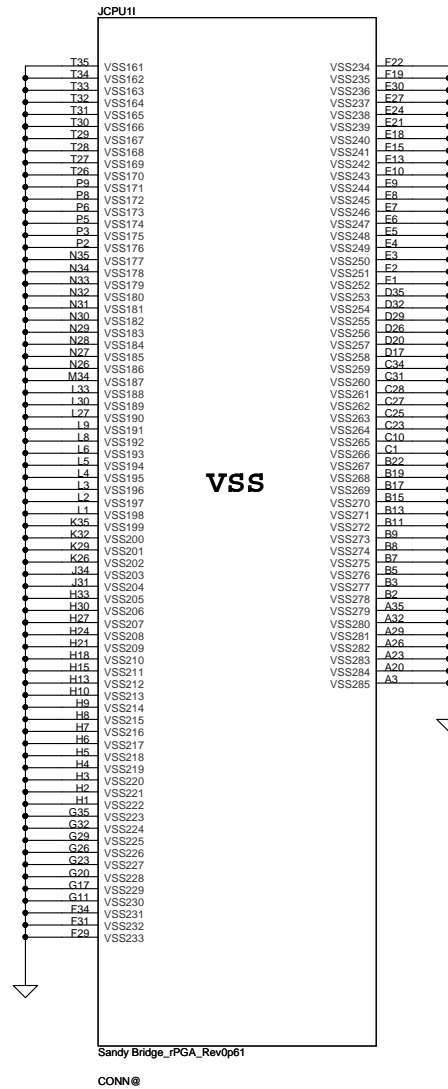
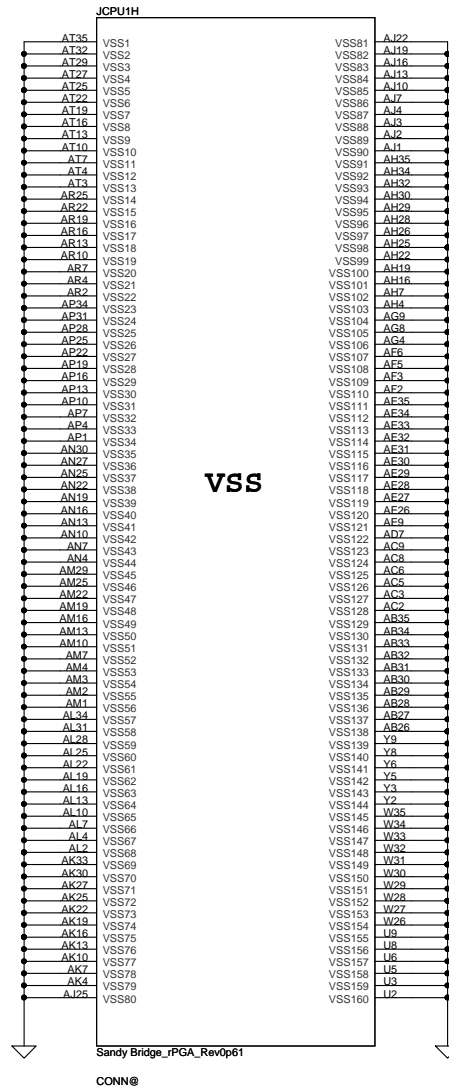
Sandy Bridge (PGA Revup01)			
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CONN@			
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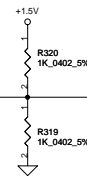
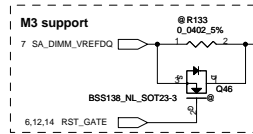
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Title	<b>PROCESSOR(5/7) PWR,BYPASS</b>		
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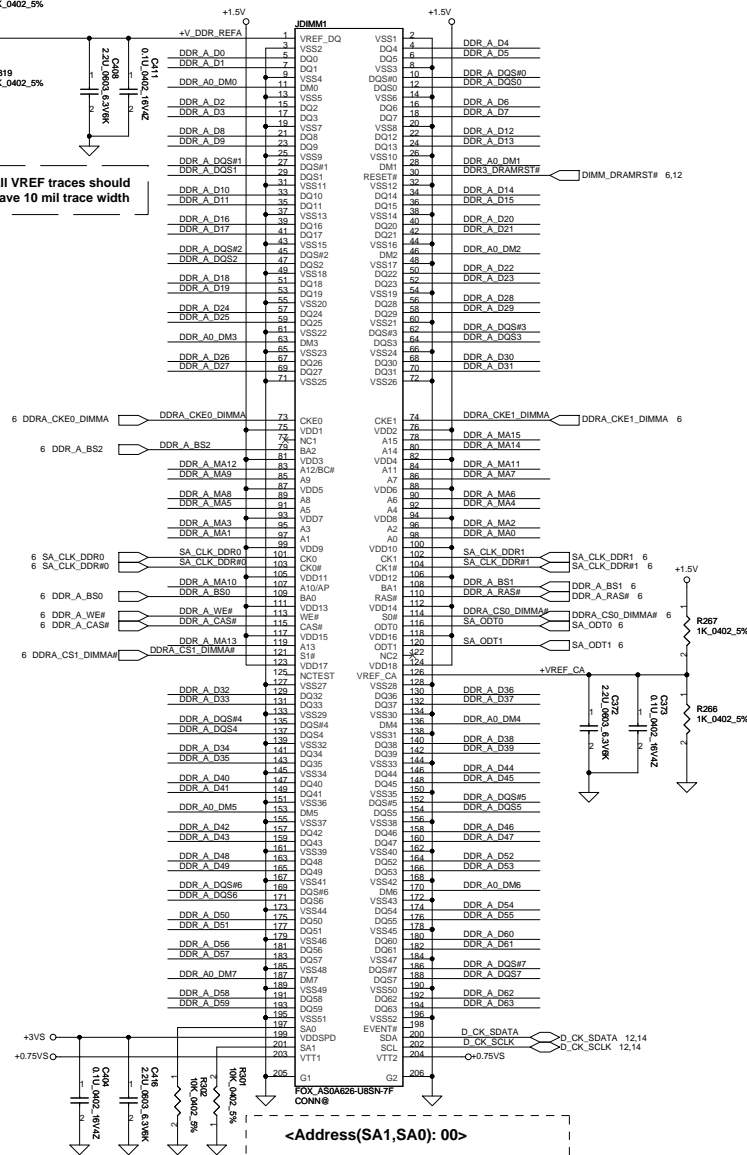




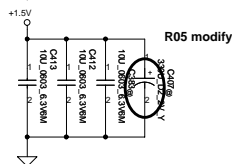
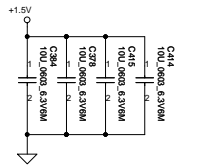
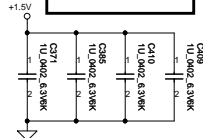
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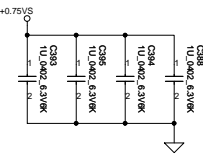
All VREF traces should have 10 mil trace width



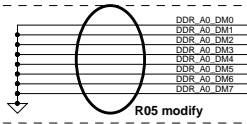
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Place near JDIMM1



R05 modify

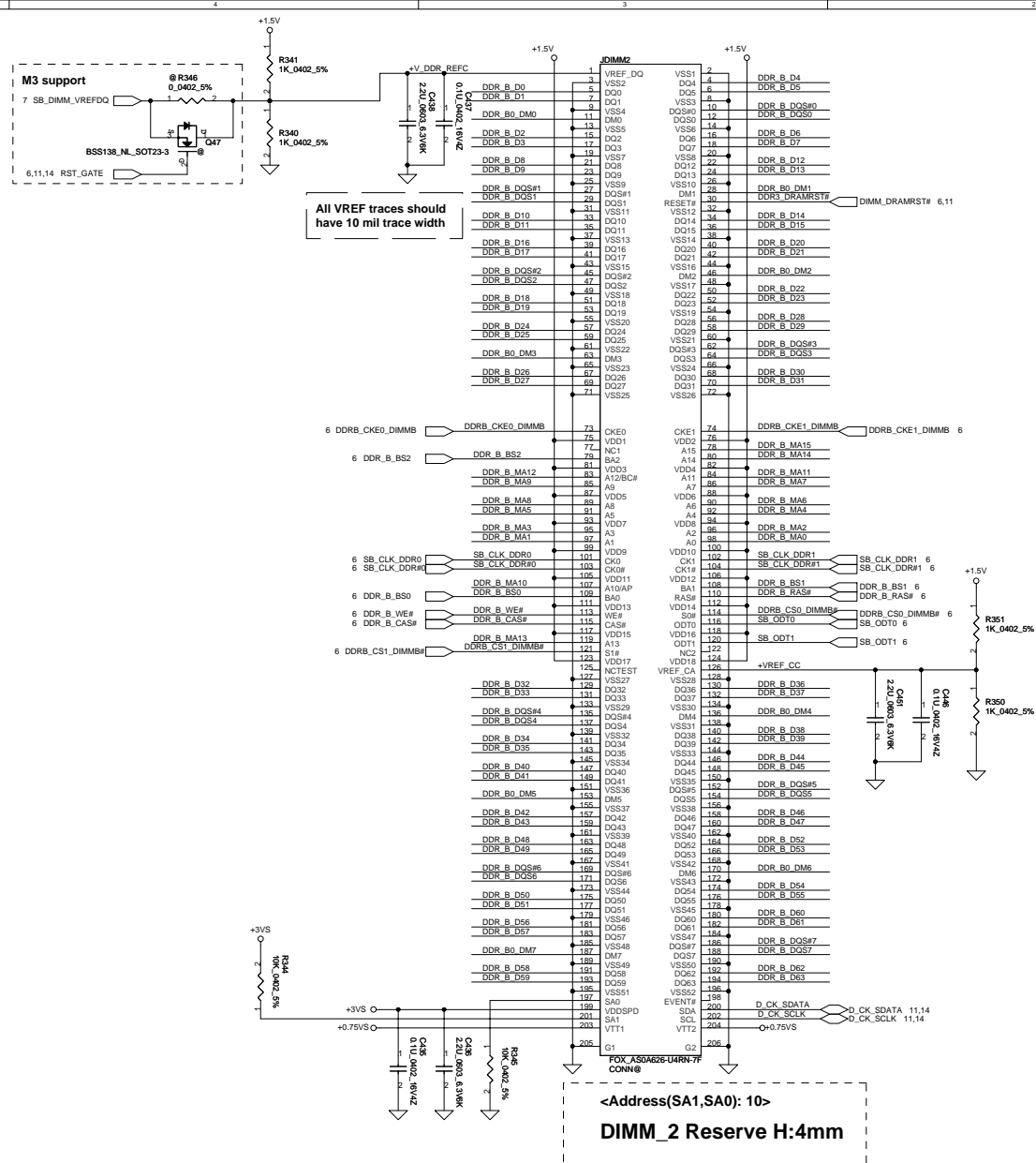


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Place near JDIMM1.203,204

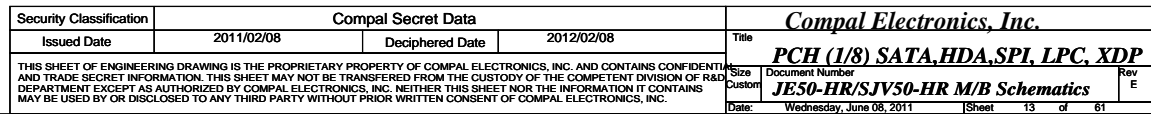


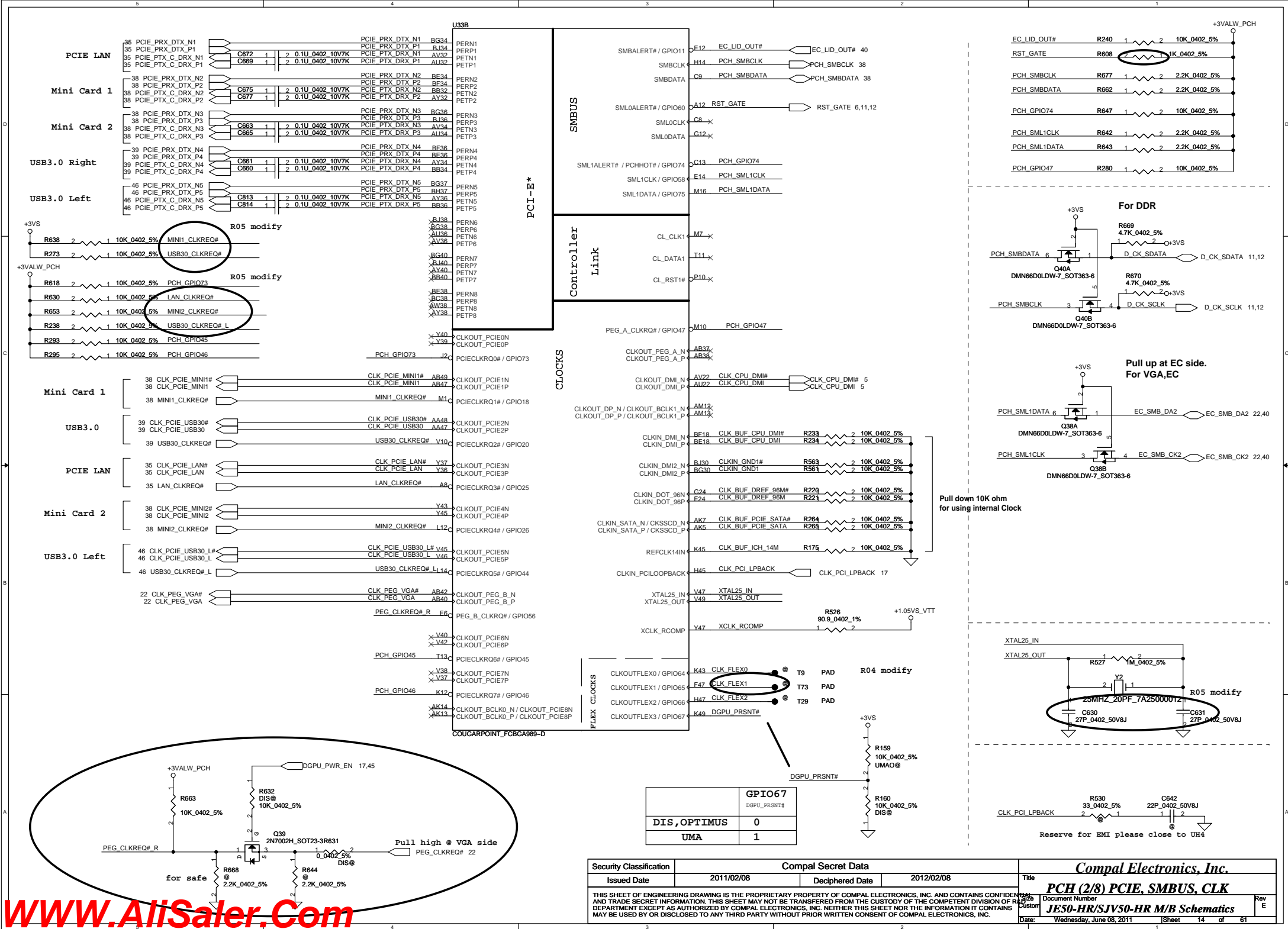
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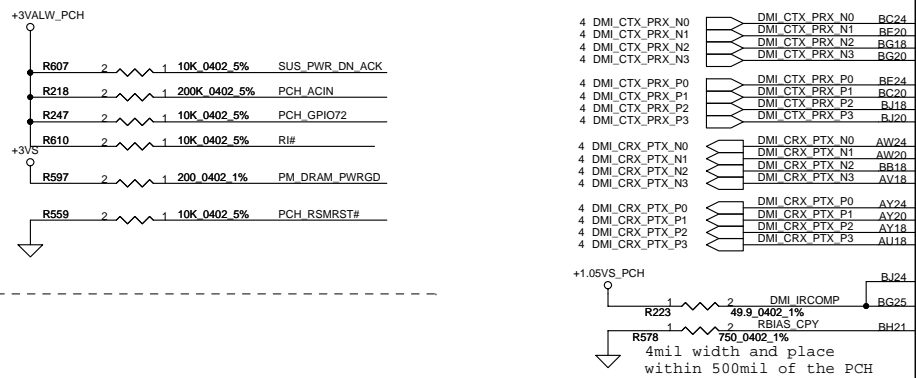
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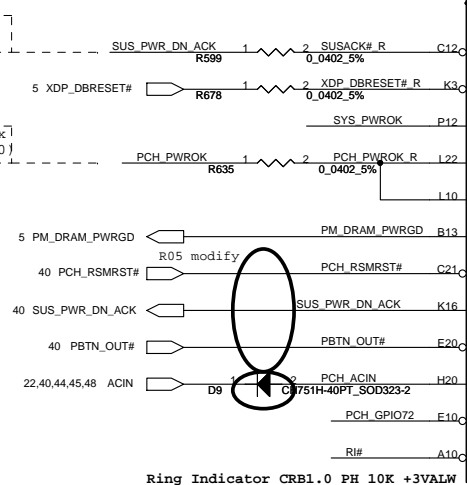






not support Deep S4,S5 mux with SUS\_PWR\_DN\_ACK

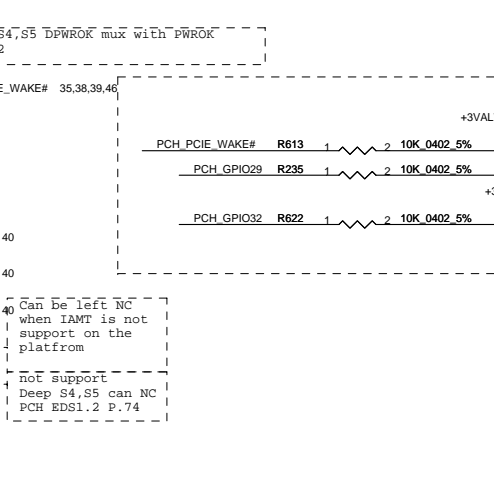
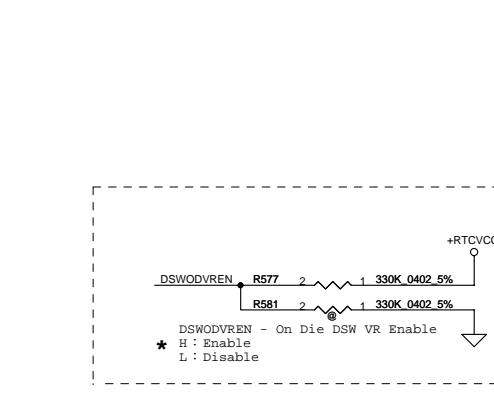
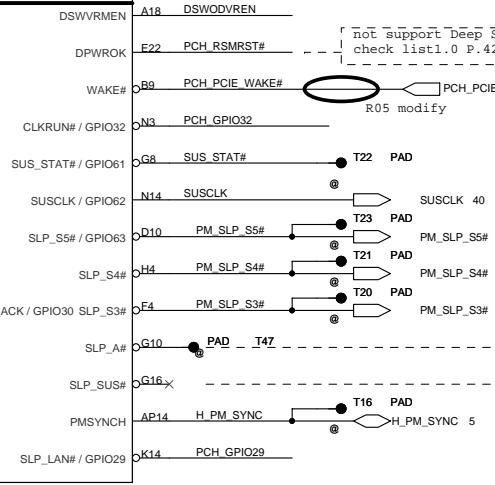
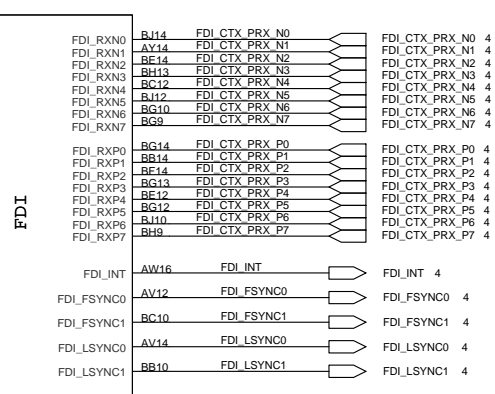
not support AMT APWROK can mux with PWROK (check list1.0 P.40)



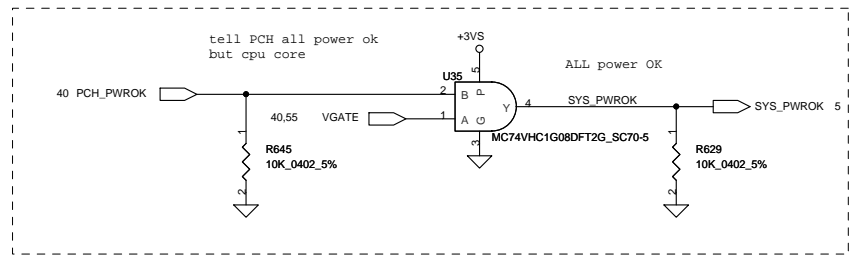
Ring Indicator CRB1.0 PH 10K +3VALW

U33C

System Power Management



Can be left NC when IAMT is not support on the platform  
not support Deep S4,S5 can NC PCH EDS1.2 P.74



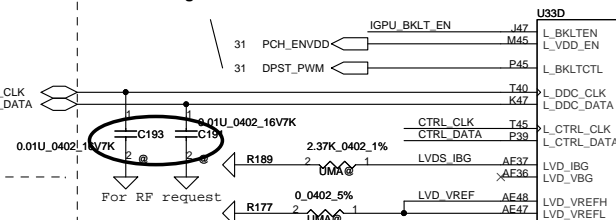
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22.40 ENBKL ← ENBKL R532 2 0.0402 5% IGPU\_BKLT\_EN  
UMA@

+3VS  
R174 1 UMA@ 2 2.2K 0402 5% CTRL\_CLK  
R158 1 UMA@ 2 2.2K 0402 5% CTRL\_DATA  
R156 1 UMA@ 2 2.2K 0402 5% PCH\_LCD\_CLK  
R157 1 UMA@ 2 2.2K 0402 5% PCH\_LCD\_DATA

+3VS  
R521 1 UMA@ 2 2.2K 0402 5% PCH\_CRT\_CLK  
R522 1 UMA@ 2 2.2K 0402 5% PCH\_CRT\_DATA  
R534 1 UMA@ 2 150 0402 1% PCH\_CRT\_B  
R533 1 UMA@ 2 150 0402 1% PCH\_CRT\_G  
R535 1 UMA@ 2 150 0402 1% PCH\_CRT\_R

Pull high at LVDS conn side.



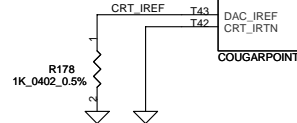
31 PCH\_TXCLK- PCH\_TXCLK- AK39  
31 PCH\_TXCLK+ PCH\_TXCLK+ AK40  
31 PCH\_TXOUT0- PCH\_TXOUT0- AN48C  
31 PCH\_TXOUT1- PCH\_TXOUT1- AM47C  
31 PCH\_TXOUT2- PCH\_TXOUT2- AE47C  
31 PCH\_TXOUT0+ PCH\_TXOUT0+ AN47  
31 PCH\_TXOUT1+ PCH\_TXOUT1+ AM49  
31 PCH\_TXOUT2+ PCH\_TXOUT2+ AK49

AE40 LVDSB\_CLK#  
AE39 LVDSB\_CLK  
AH45C LVDSB\_DATA#0  
AH47C LVDSB\_DATA#1  
AE49C LVDSB\_DATA#2  
AE45C LVDSB\_DATA#3  
AH43 LVDSB\_DATA0  
AH49 LVDSB\_DATA1  
AE47 LVDSB\_DATA2  
AE43 LVDSB\_DATA3

32 PCH\_CRT\_B PCH\_CRT\_B N48  
32 PCH\_CRT\_G PCH\_CRT\_G P49  
32 PCH\_CRT\_R PCH\_CRT\_R T49

32 PCH\_CRT\_CLK PCH\_CRT\_CLK T39  
32 PCH\_CRT\_DATA PCH\_CRT\_DATA M40

32 PCH\_CRT\_HSYNC CRT\_HSYNC M47  
32 PCH\_CRT\_VSYNC CRT\_VSYNC M49



LVDS

CRT

Digital Display Interface

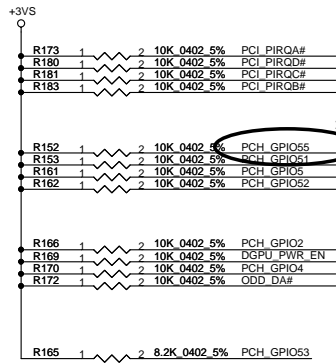
SDVO\_TVCLKINN AP43  
SDVO\_TVCLKINP AP45  
SDVO\_STALLN AM42  
SDVO\_STALLP AM40  
SDVO\_INTN AP39  
SDVO\_INTP AP40  
SDVO\_CTRLCLK P38  
SDVO\_CTRLDATA M39  
SDVO\_SCLK SDVO\_SCLK 33  
SDVO\_SDATA SDVO\_SDATA 33  
DDPB\_AUXN AT49  
DDPB\_AUXP AT47  
DDPB\_HPDP AT40  
PCH\_DPB\_HPDP PCH\_DPB\_HPDP 33  
DDPB\_0N AV42  
DDPB\_0P AV40  
DDPB\_1N AV45  
DDPB\_1P AV46  
DDPB\_2N AU48  
DDPB\_2P AU47  
DDPB\_3N AV47  
DDPB\_3P AV49  
DDPC\_CTRLCLK P46  
DDPC\_CTRLDATA P47  
DDPC\_AUXN AP41  
DDPC\_AUXP AP43  
DDPC\_HPDP AT38  
DDPC\_0N AY41  
DDPC\_0P AY43  
DDPC\_1N AY45  
DDPC\_1P AY46  
DDPC\_2N BA42  
DDPC\_2P BA43  
DDPC\_3N BB47  
DDPC\_3P BB49  
DDPD\_CTRLCLK M43  
DDPD\_CTRLDATA M36  
DDPD\_AUXN AT45  
DDPD\_AUXP AT43  
DDPD\_HPDP BH41  
DDPD\_0N BB43  
DDPD\_0P BB45  
DDPD\_1N BF44  
DDPD\_1P BF44  
DDPD\_2N BF44  
DDPD\_2P BF44  
DDPD\_3N BJ42  
DDPD\_3P BG42

SDVO\_CTRLDATA strap pull high at level shift page

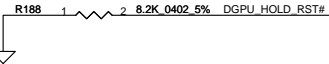
HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/02/08	Deciphered Date	2012/02/08	Title	PCH (4/9) LVDS,CRT,DP,HDMI
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				Rev	E



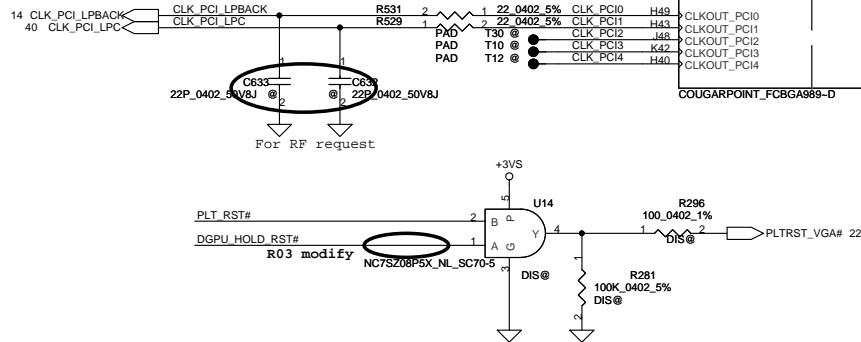


R03 modify



#### GPIO51 Internal pull high

Boot BIOS Strap bit1 BBS1		
Boot BIOS		
Bit11	Bit10	Destination
GNT1# / GPIO51	0	Reserved
	1	PCI
	1	SPI
	0	LPC



U33E

TP1  
TP2  
TP3  
TP4  
TP5  
TP6  
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TP36  
TP37  
TP38  
TP39  
TP40

RSVD

PCI

USB

PIROA#  
PIROB#  
PIROC#  
PIROD#  
REQ1# / GPIO50  
REQ2# / GPIO52  
REQ3# / GPIO54  
GNT1# / GPIO51  
GNT2# / GPIO53  
GNT3# / GPIO55  
PIROE# / GPIO2  
PIROF# / GPIO3  
PIROG# / GPIO4  
PIROH# / GPIO5

COUGARPOINT\_FCBGA989-D

NV\_CE#0  
NV\_CE#1  
NV\_CE#2  
NV\_CE#3  
NV\_DQ0  
NV\_DQ1  
NV\_DQ2  
NV\_DQ3  
NV\_DQ4  
NV\_DQ5  
NV\_DQ6  
NV\_DQ7  
NV\_DQ8  
NV\_DQ9  
NV\_DQ10  
NV\_DQ11  
NV\_DQ12  
NV\_DQ13  
NV\_DQ14  
NV\_DQ15  
NV\_ALE  
NV\_CLE  
NV\_RCOMP  
NV\_RB#  
NV\_RE#\_WRB0  
NV\_RE#\_WRB1  
NV\_WE#\_CK0  
NV\_WE#\_CK1

NVRAM

USB20\_N0  
USB20\_P0  
USB20\_N1  
USB20\_P1  
USB20\_N2  
USB20\_P2  
USB20\_N3  
USB20\_P3  
USB20\_N8  
USB20\_P8  
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USB20\_N13  
USB20\_P13

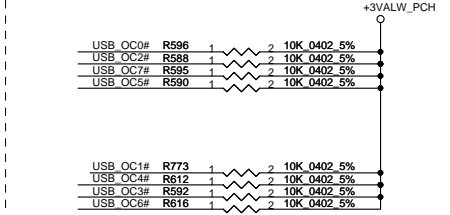
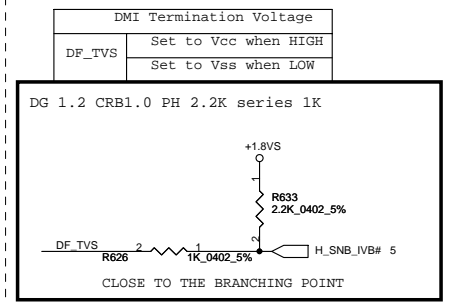
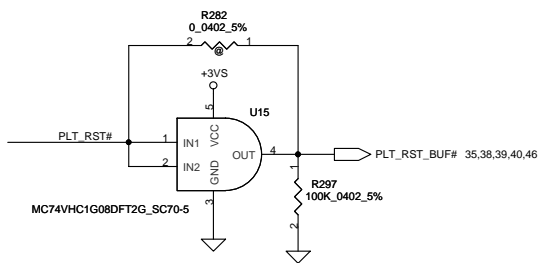
Some PCH config not support USB port 6 & 7.

Mini Card 1 (WLAN)  
3G/B (WWAN)  
CMOS Camera (LVDS)  
Mini2 Card 2 (Reserved)  
3G/B (SIM Card)  
BlueTooth

Within 500 mils

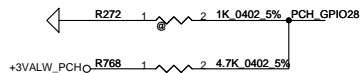
R03 modify

USB\_OC0#  
USB\_OC1#  
USB\_OC2#  
USB\_OC3#  
USB\_OC4#  
USB\_OC5#  
USB\_OC6#  
USB\_OC7#

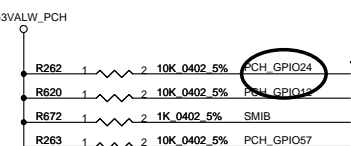
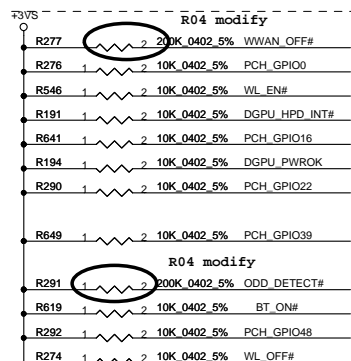
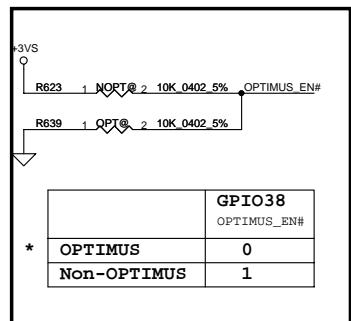
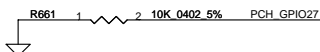


GPIO28 HDA\_SYNC PH(PLL +=1.5VS)  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up

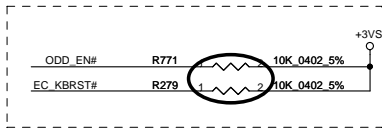
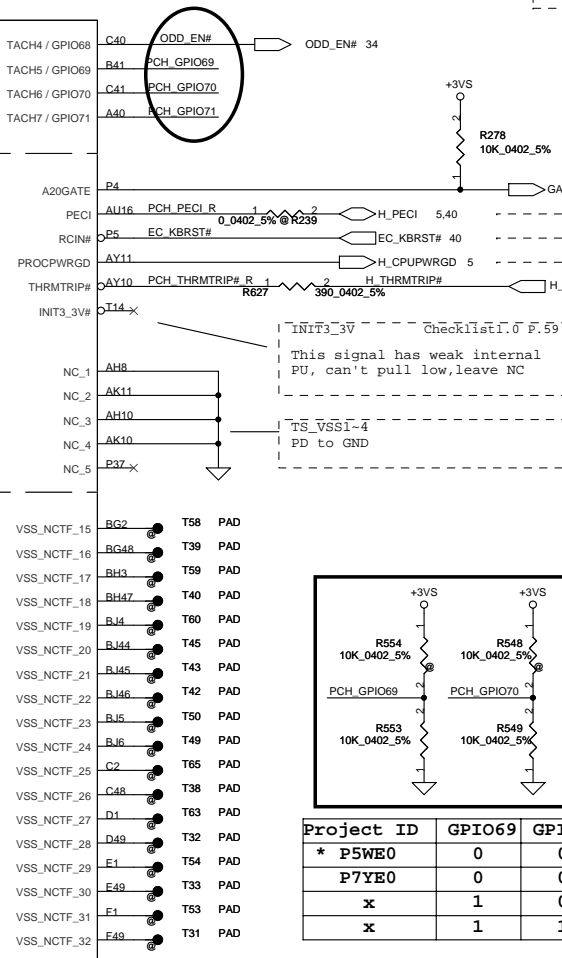
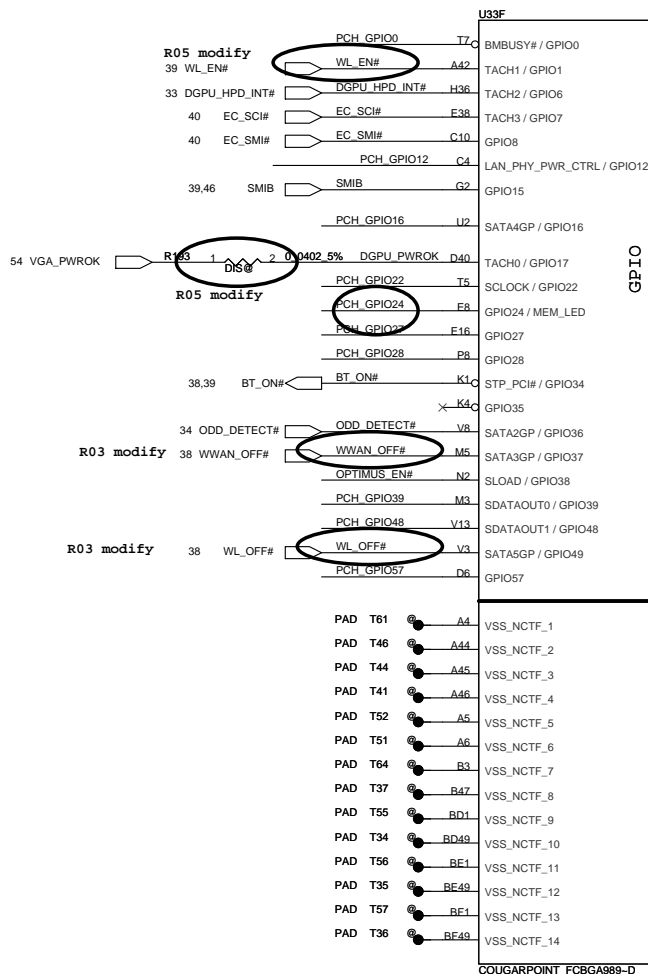
\* H: On-Die voltage regulator enable  
L: On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal  
RTC alarm,Power BTN,GPIO27  
PCH\_GPIO27 (Have internal Pull-High)  
Deep S4,S5 wake event signal  
No use PD to GND Check list1.0 P.70

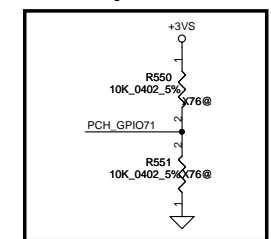
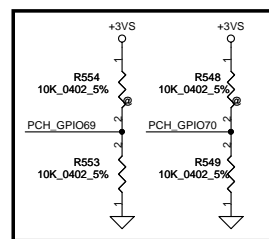


GPIO24 Unmultiplexed  
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.  
CRB1.0 PH10K to +3VALW



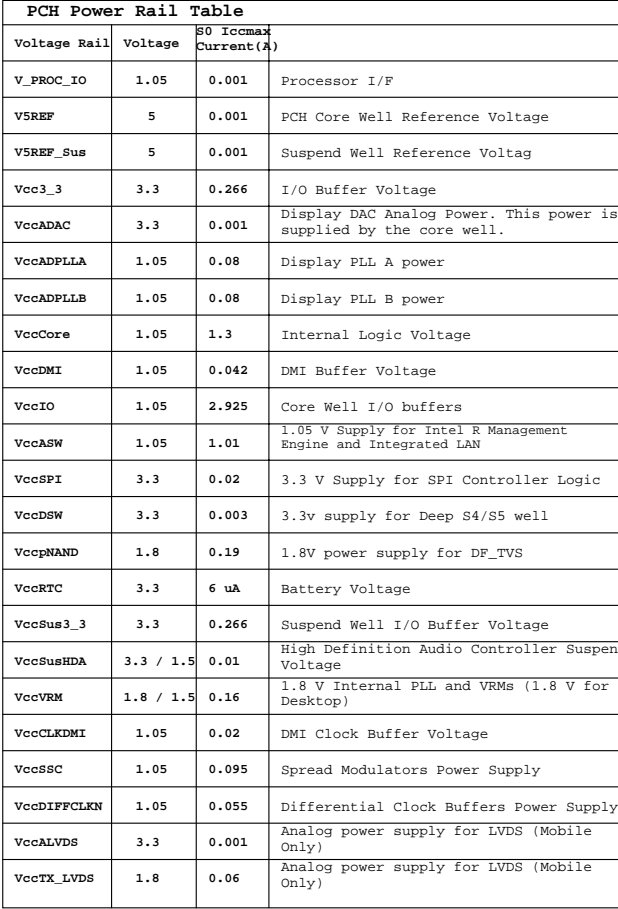
PECI CPU-EC  
CTRL+ALT+DEL  
non CPU power ok  
130 degree  
shut down

INIT3\_3V  
This signal has weak internal PU, can't pull low, leave NC  
TS\_VSSI-4  
PD to GND

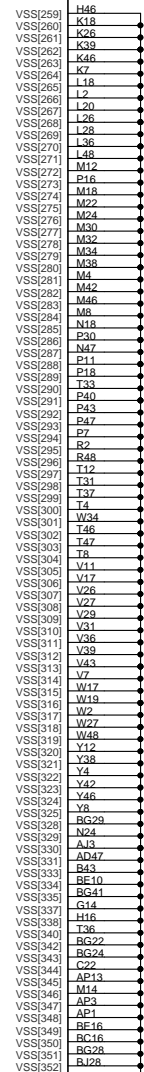
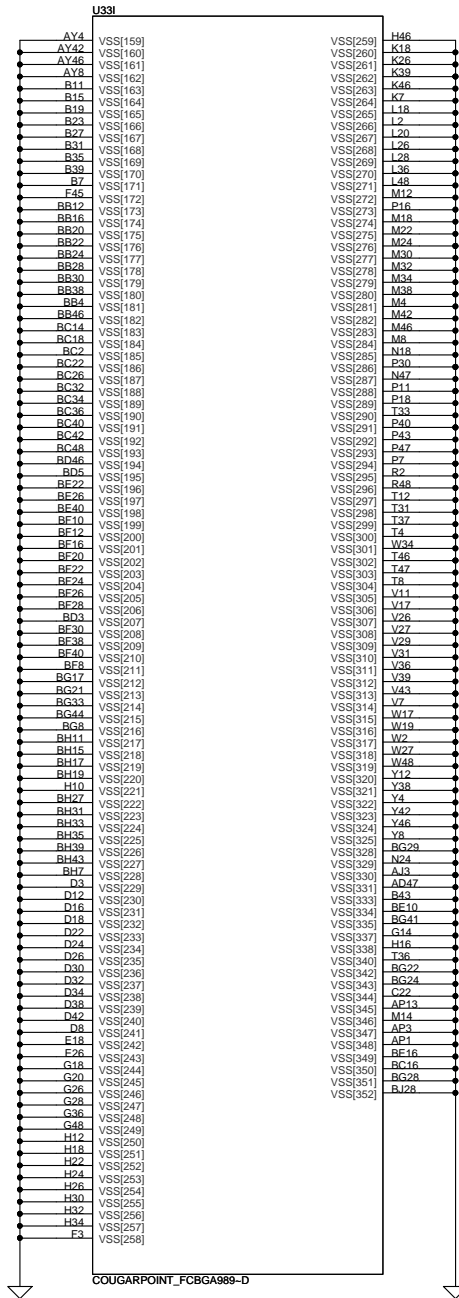
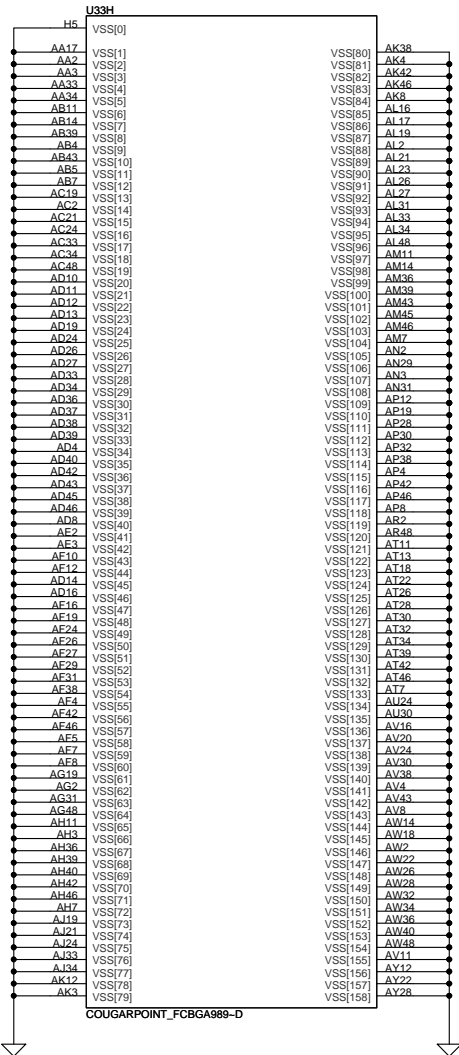


Project ID	GPIO69	GPIO70
* P5WE0	0	0
P7YE0	0	0
x	1	0
x	1	1

	GPIO71
	PCH_GPIO71
*VRAM 800 MHz	0
VRAM 900 MHz	1







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4 PEG\_HTX\_C.GRX\_P0  
4 PEG\_HTX\_C.GRX\_N0  
4 PEG\_HTX\_C.GRX\_P1  
4 PEG\_HTX\_C.GRX\_N1  
4 PEG\_HTX\_C.GRX\_P2  
4 PEG\_HTX\_C.GRX\_N2  
4 PEG\_HTX\_C.GRX\_P3  
4 PEG\_HTX\_C.GRX\_N3  
4 PEG\_HTX\_C.GRX\_P4  
4 PEG\_HTX\_C.GRX\_N4  
4 PEG\_HTX\_C.GRX\_P5  
4 PEG\_HTX\_C.GRX\_N5  
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4 PEG\_GTX\_HRX\_N15

AP17 PEX\_TX0  
AN17 PEX\_TX0\_N  
AP18 PEX\_TX1  
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AN19 PEX\_TX2\_N  
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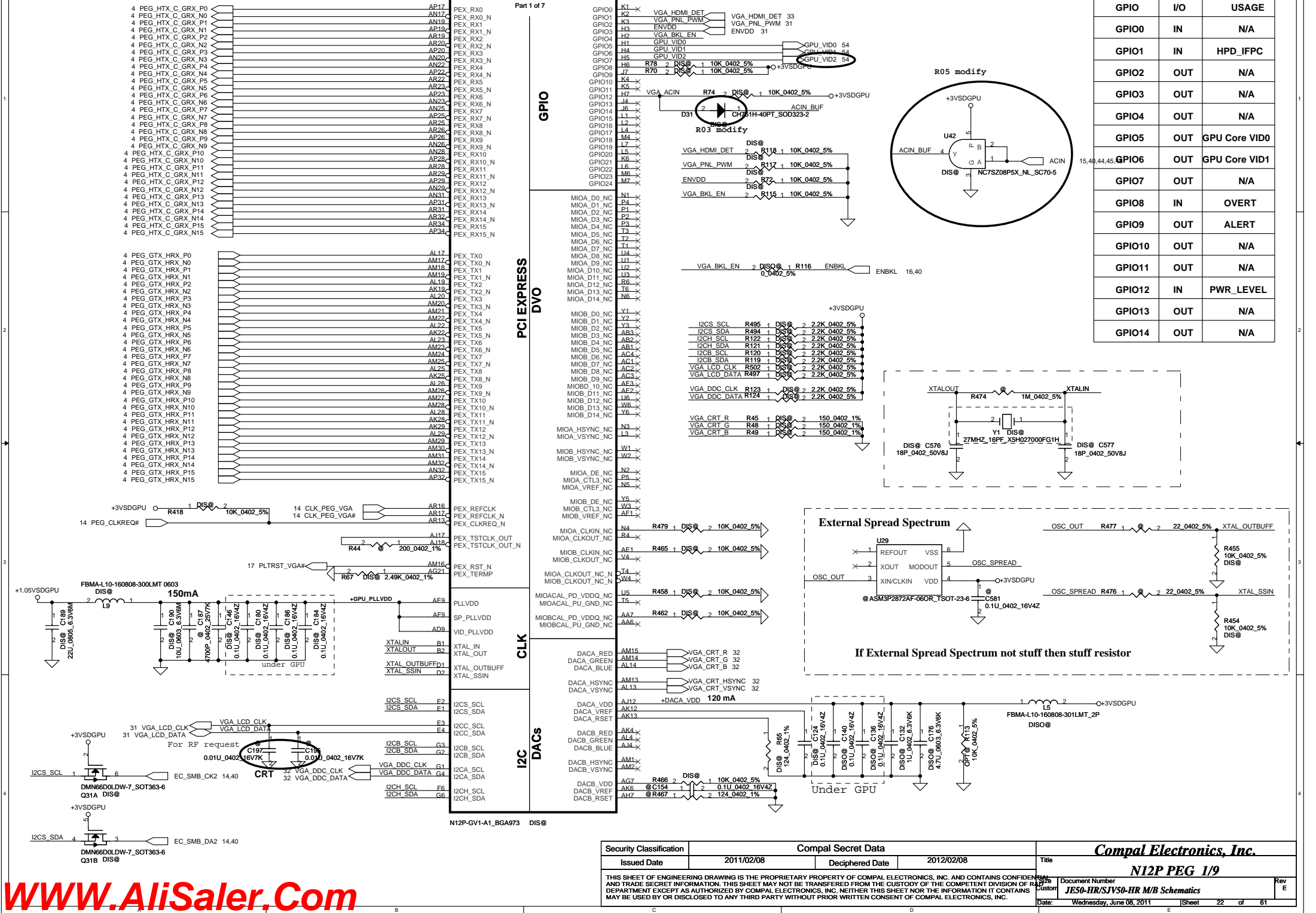
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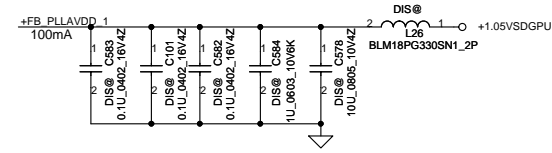
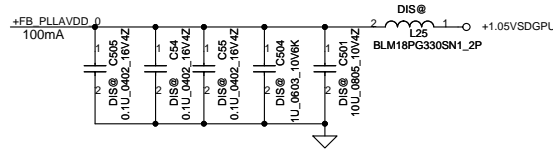
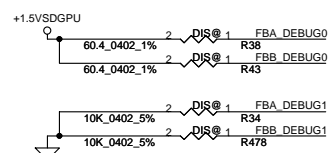
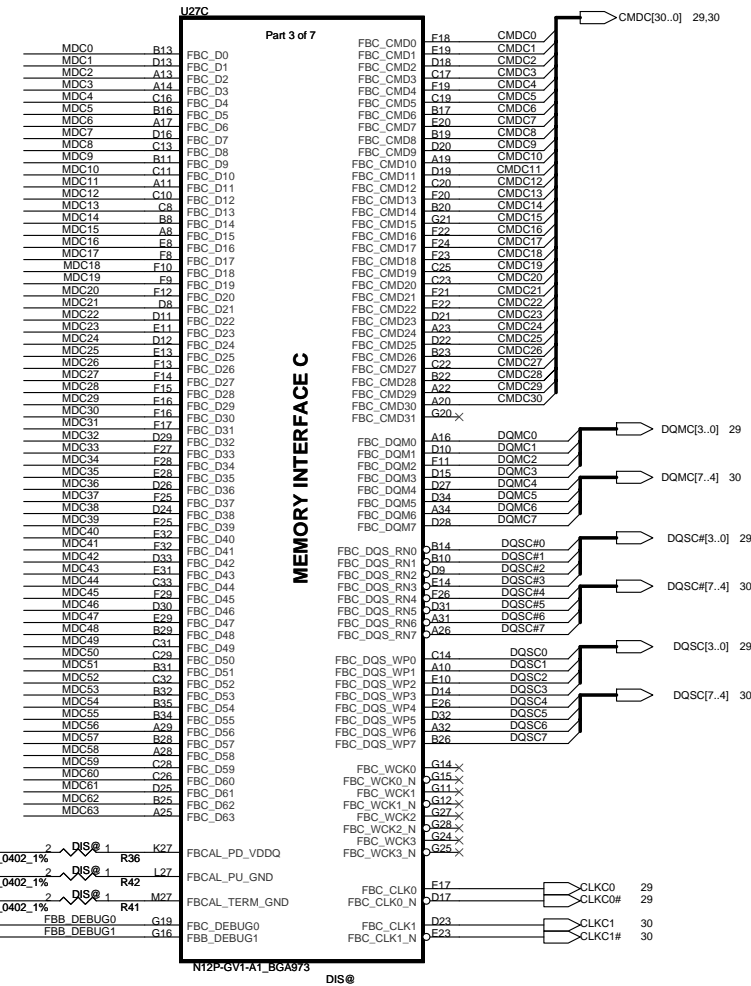
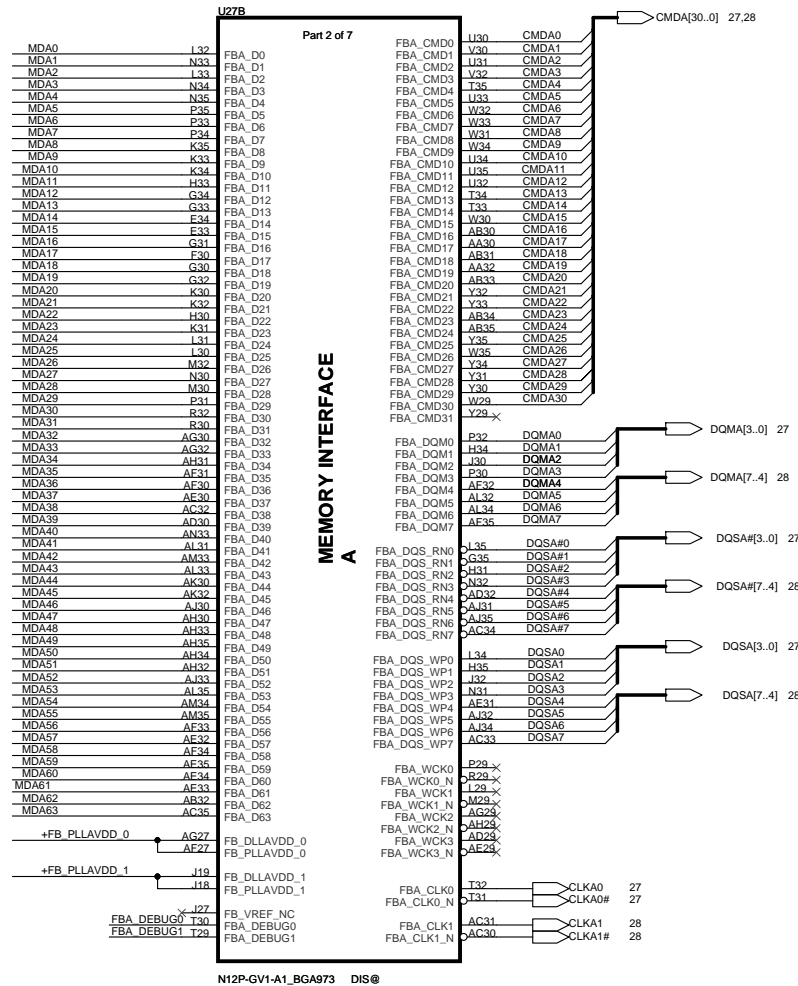
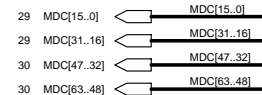
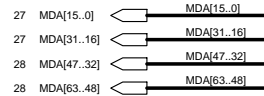
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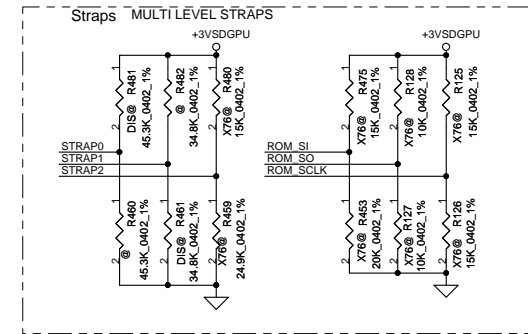
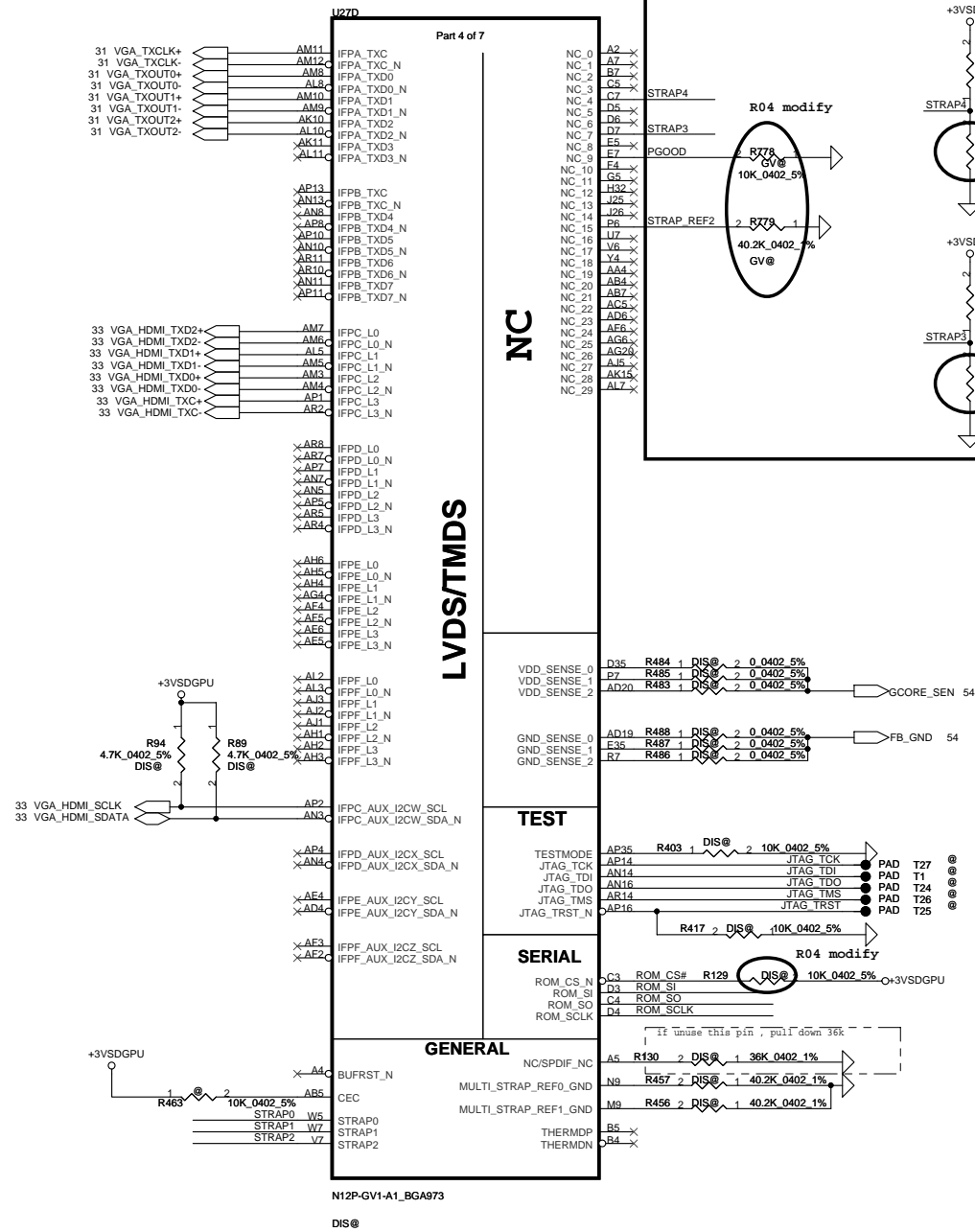


# VRAM Interface



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For GB2-128 & GB2b-128 colayout....



For N12P-GS strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
W12P-GS	800 MHz	64M* 16* 8 1GB	Hynix SA0000032420	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 5K	R127 PD 10K	R125 PU 15K
W12P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 15K	R127 PD 10K	R125 PU 15K
W12P-GS	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS10	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 20K	R127 PD 10K	R125 PU 15K
W12P-GS	800 MHz	128M* 16* 8 2GB	Samsung SA00003MQ60	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 45K	R127 PD 10K	R125 PU 15K
W12P-GS	800 MHz	128M* 16* 8 2GB	Hynix SA000003VS10	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 35K	R127 PD 10K	R125 PU 15K

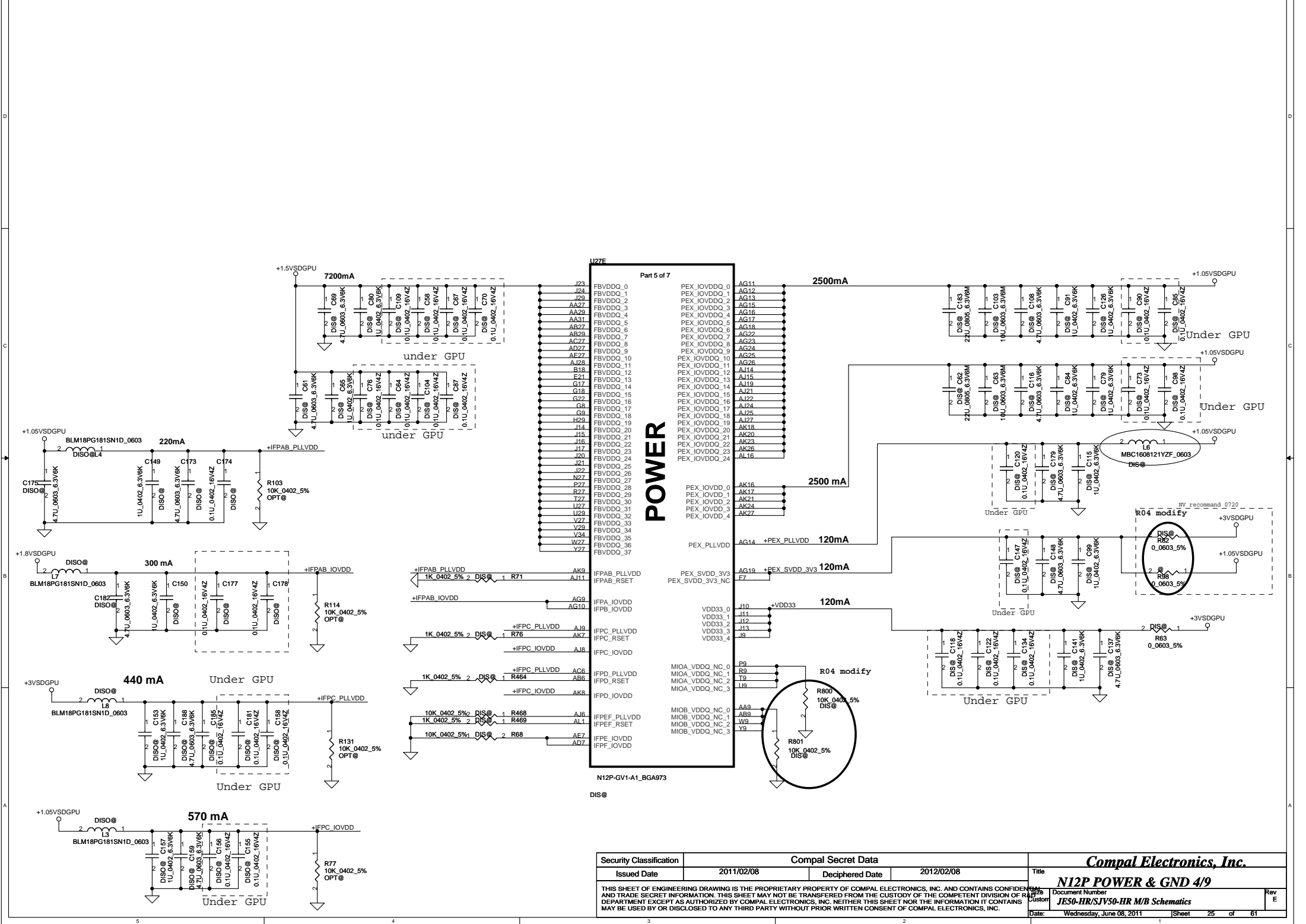
For N12P-GV (ES) strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GV(ES)	800 MHz	64M* 16" 4 512MB	Hynix SA0000032420	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 5K	R128 PU 10K	R125 PU 15K
N12P-GV(ES)	900 MHz	64M* 16" 4 512MB	SA0000041S40	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 15K	R128 PU 10K	R125 PU 15K
N12P-GV(ES)	900 MHz	64M* 16" 4 512MB	Samsung SA00004GS10	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 20K	R128 PU 10K	R125 PU 15K
N12P-GV(ES)	800 MHz	128M* 16" 4 1GB	Hynix SA00003M060	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 45K	R128 PU 10K	R125 PU 15K
N12P-GV(ES)	800 MHz	128M* 16" 4 1GB	Hynix SA00003VS10	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 35K	R128 PU 10K	R125 PU 15K

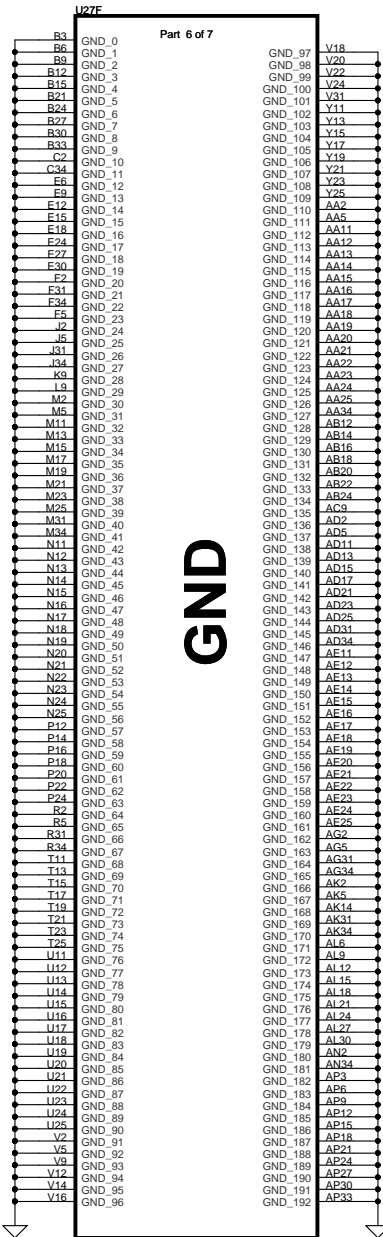
For N12P-GV-OP-B-A1 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GV OP-B-A1	800 MHz	64M* 16* 4 512MB	Hynix SA000032420	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 5K	R128 PU 10K	R125 PU 5K
N12P-GV OP-B-A1	900 MHz	64M* 16* 4 512MB	Hynix SA000041540	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 15K	R128 PU 10K	R125 PU 5K
N12P-GV OP-B-A1	900 MHz	64M* 16* 4 512MB	Samsung SA00004GS10	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 20K	R128 PU 10K	R125 PU 5K
N12P-GV OP-B-A1	800 MHz	128M* 16* 4 1GB	Samsung SA00003MQ060	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 45K	R128 PU 10K	R125 PU 5K
N12P-GV OP-B-A1	800 MHz	128M* 16* 4 1GB	Hynix SA00003VS10	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 35K	R128 PU 10K	R125 PU 5K



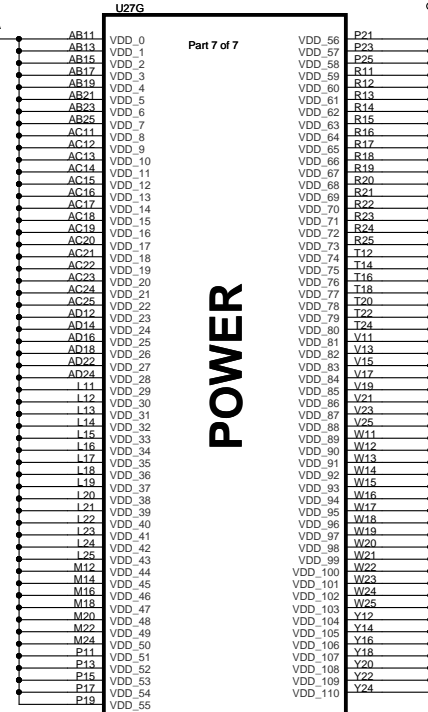
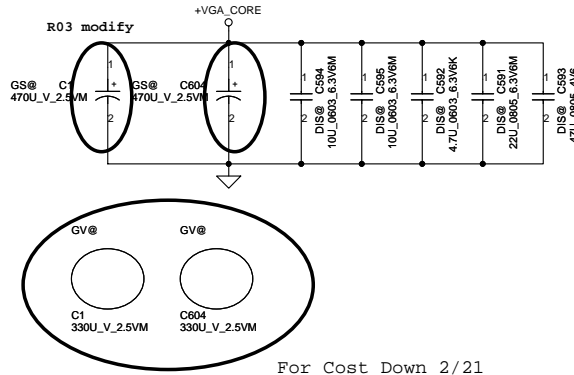
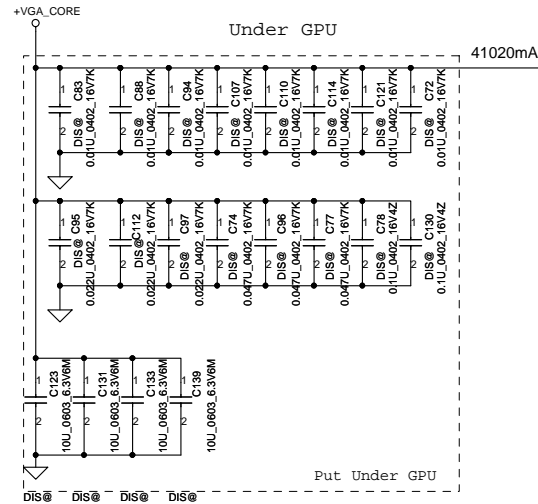


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N12P-GV1-A1\_BGA973

DIS@



N12P-GV1-A1\_BGA973

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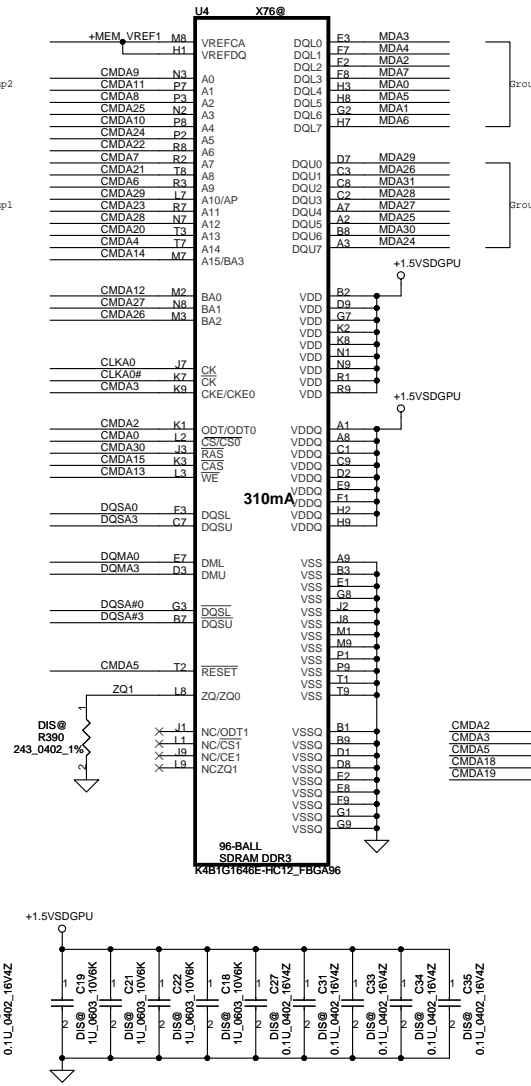
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N12P POWER & GND 5/9

Rev E

**64Mx16 DDR3 \*8==>1GB**

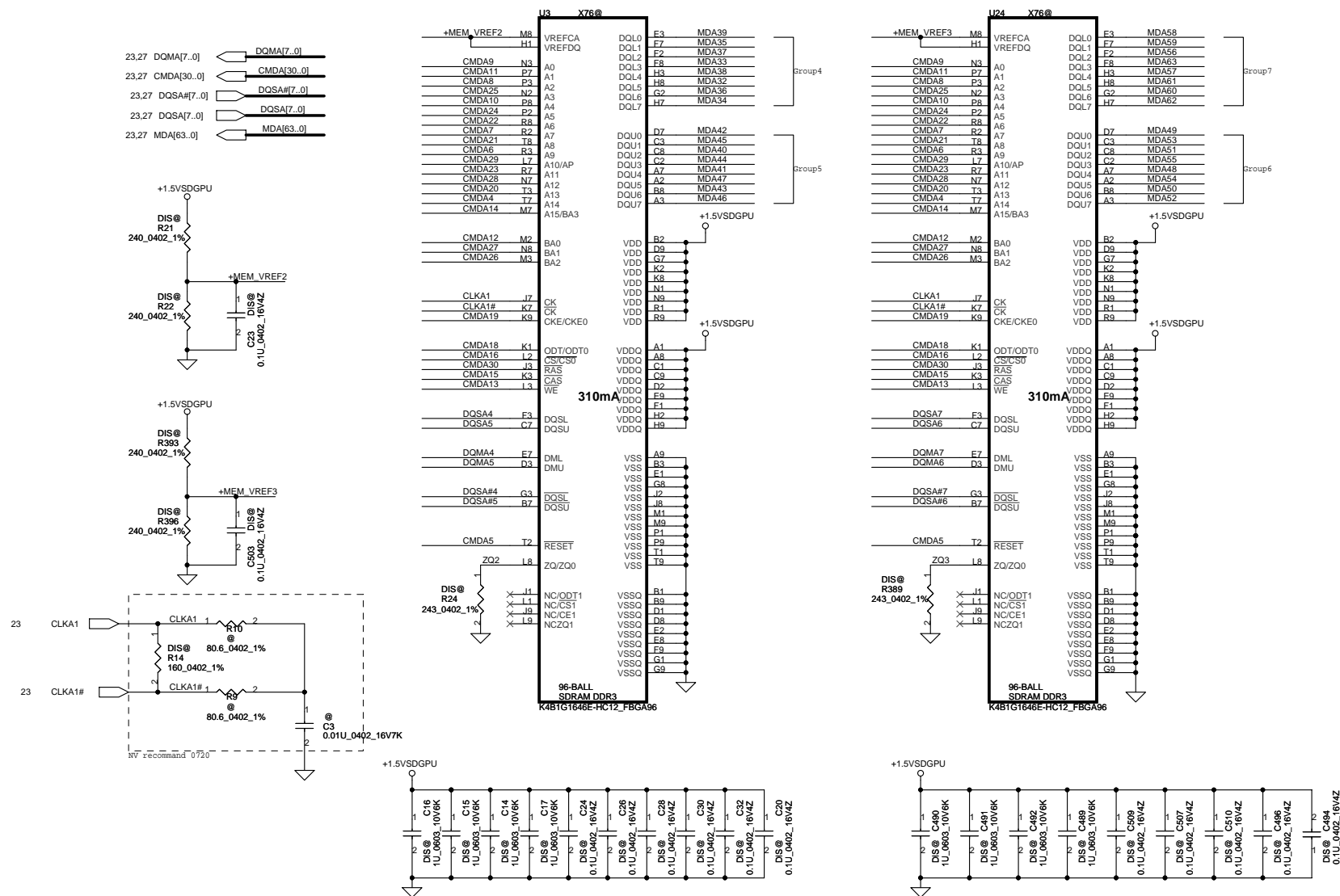


	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

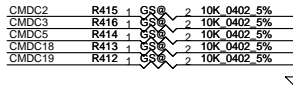
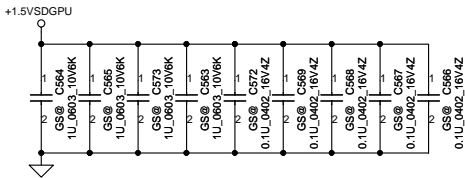
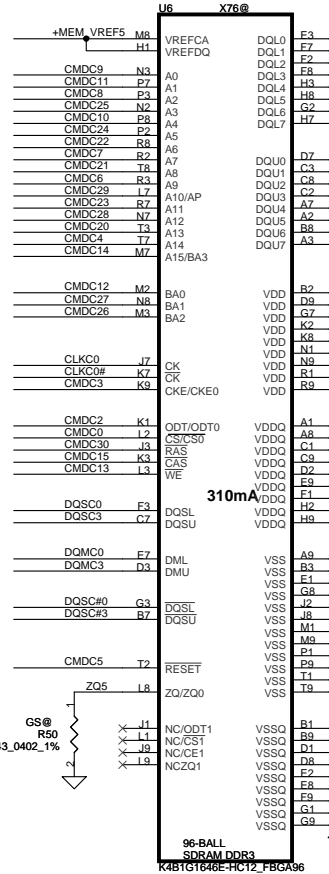
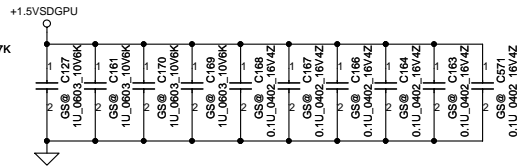
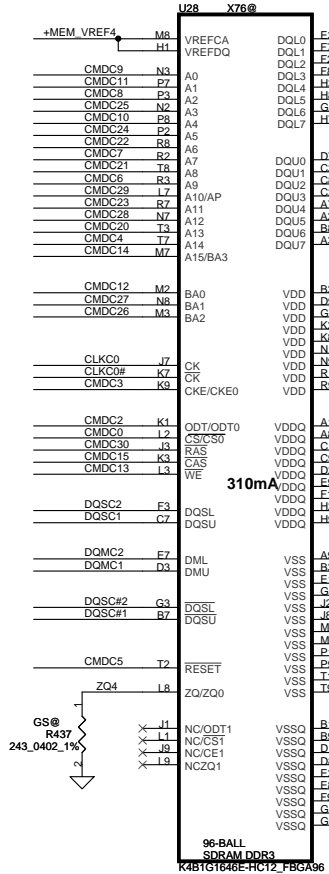
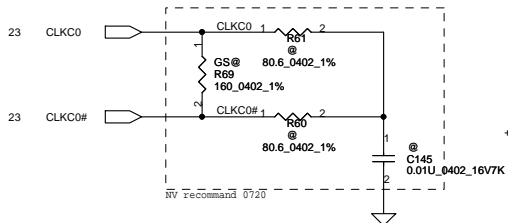
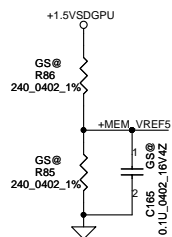
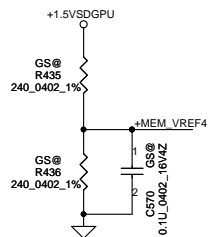
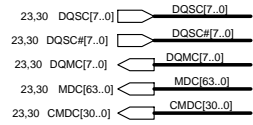


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*

LOW HIGH

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

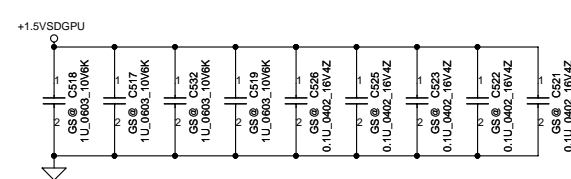
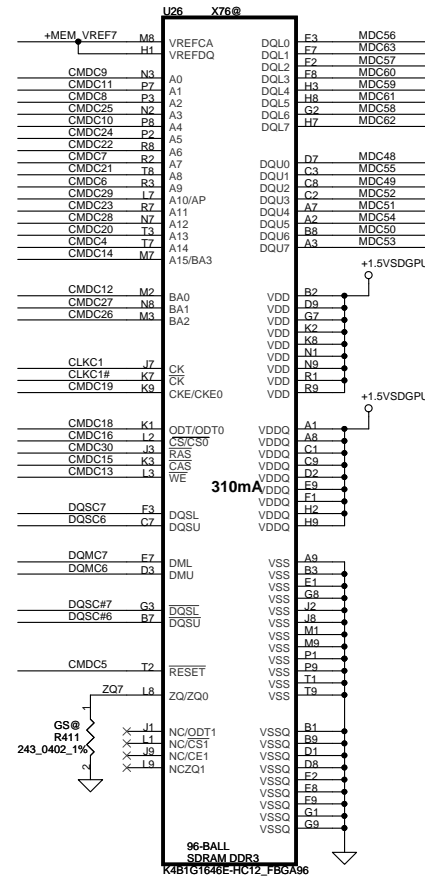
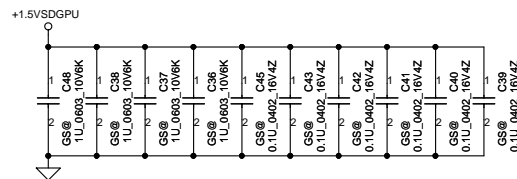
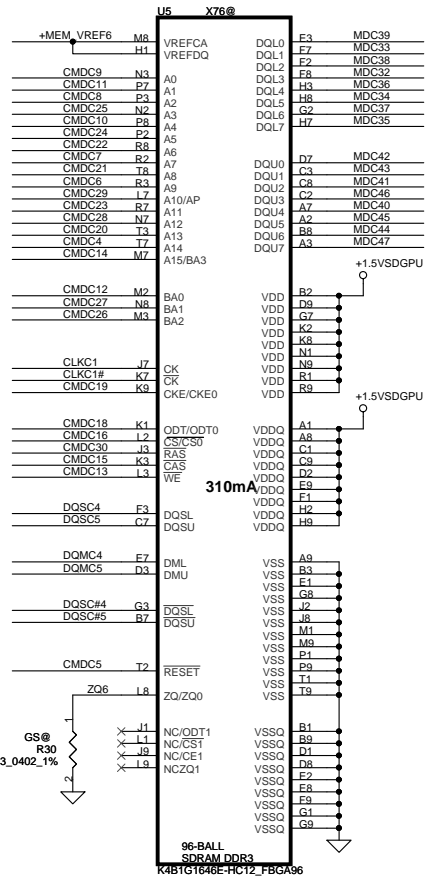
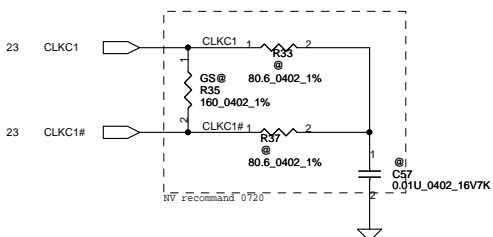
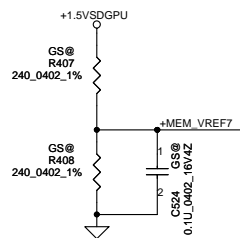
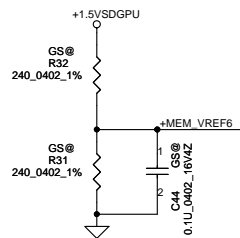
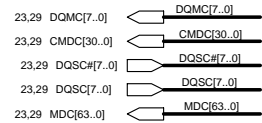


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

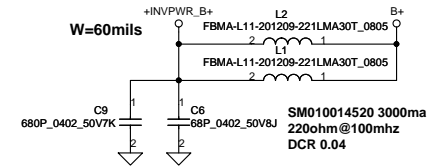
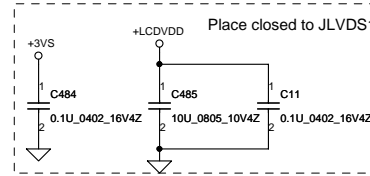
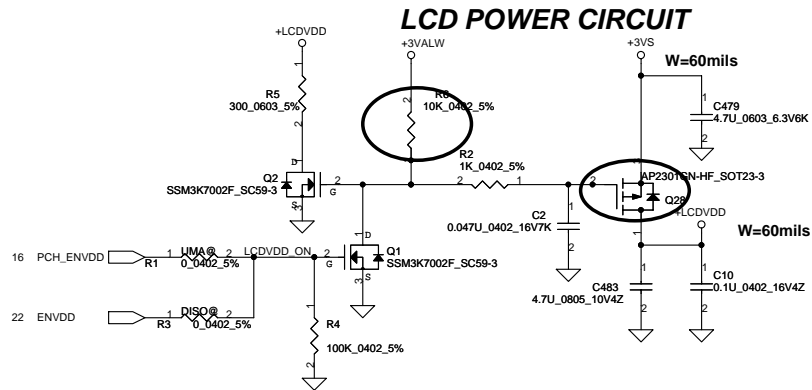
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

**64Mx16 DDR3 \*8==>1GB**

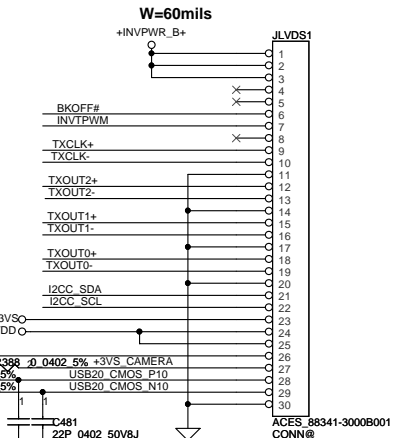


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

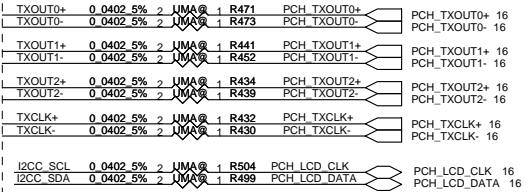
LOW HIGH



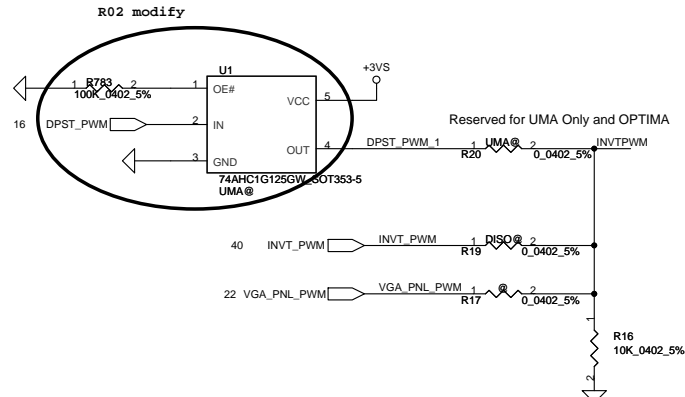
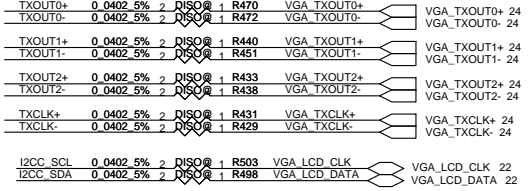
### LCD/LED PANEL Conn.



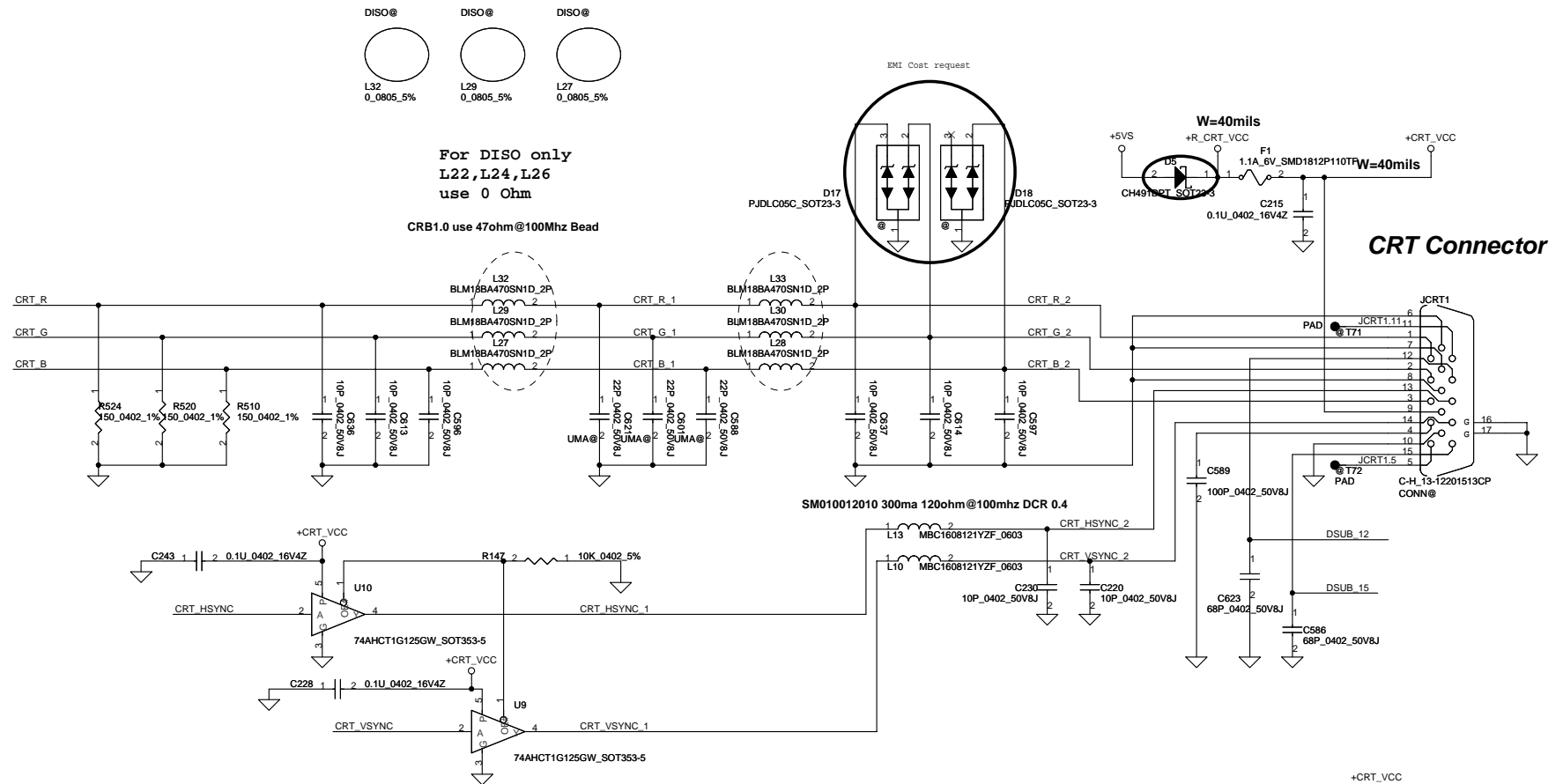
### UMA Only / Optimus



### Discrete ONLY



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Issued Date				2011/02/08				Title			
Deciphered Date				2012/02/08				LVDS Connector			
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Date: Wednesday, June 08, 2011				Sheet				31 of 81			



#### UMA Only / OPTIMUS

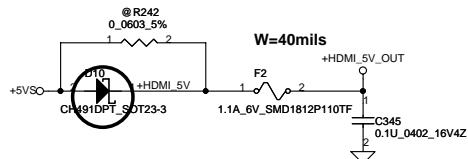
16	PCH_CRT_R	PCH_CRT_R	R420	UMA	1	0.0402_5%	CRT_R
16	PCH_CRT_G	PCH_CRT_G	R424	UMA	1	0.0402_5%	CRT_G
16	PCH_CRT_B	PCH_CRT_B	R422	UMA	1	0.0402_5%	CRT_B
16	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R428	UMA	1	33_0402_5%	CRT_HSYNC
16	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R426	UMA	1	33_0402_5%	CRT_VSYNC
16	PCH_CRT_CLK	PCH_CRT_CLK	R506	UMA	1	0.0402_5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH_CRT_DATA	R501	UMA	1	0.0402_5%	CRT_DDC_DATA

#### Discrete only

22	VGA_CRT_R	VGA_CRT_R	R419	DISO	1	0.0402_5%	CRT_R
22	VGA_CRT_G	VGA_CRT_G	R423	DISO	1	0.0402_5%	CRT_G
22	VGA_CRT_B	VGA_CRT_B	R421	DISO	1	0.0402_5%	CRT_B
22	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R427	DISO	1	0.0402_5%	CRT_HSYNC
22	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R425	DISO	1	0.0402_5%	CRT_VSYNC
22	VGA_DDC_CLK	VGA_DDC_CLK	R505	DISO	1	0.0402_5%	CRT_DDC_CLK
22	VGA_DDC_DATA	VGA_DDC_DATA	R500	DISO	1	0.0402_5%	CRT_DDC_DATA

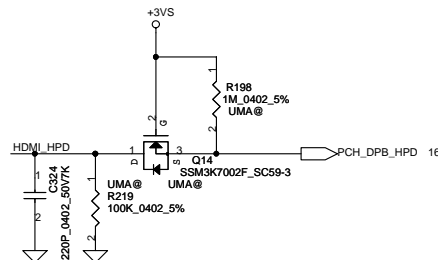
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/02/08	Deciphered Date	2012/02/08	Title	CRT Connector
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				Date	Wednesday, June 08, 2011
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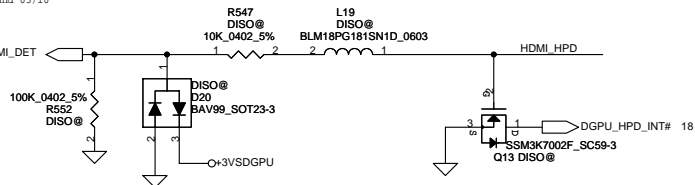


UMA	16 PCH_DPB_N0	C280	UMA@	2	1	0.1U_0402_10V7K	HDMI TX2-
	16 PCH_DPB_P0	C281	UMA@	2	1	0.1U_0402_10V7K	HDMI TX2+
DIS	16 PCH_DPB_N1	C283	UMA@	2	1	0.1U_0402_10V7K	HDMI TX1-
	16 PCH_DPB_P1	C282	UMA@	2	1	0.1U_0402_10V7K	HDMI TX1+
DIS	16 PCH_DPB_N2	C287	UMA@	2	1	0.1U_0402_10V7K	HDMI TX0-
	16 PCH_DPB_P2	C286	UMA@	2	1	0.1U_0402_10V7K	HDMI TX0+
DIS	16 PCH_DPB_N3	C285	UMA@	2	1	0.1U_0402_10V7K	HDMI CLK-
	16 PCH_DPB_P3	C284	UMA@	2	1	0.1U_0402_10V7K	HDMI CLK+

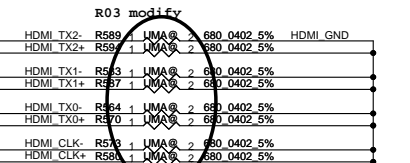
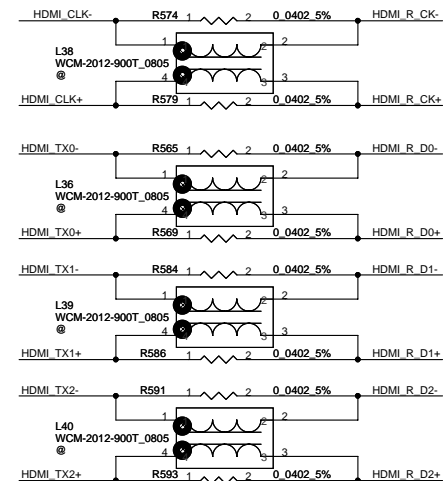
DIS	24 VGA_HDMI_TXD2-	C234	DISO@	1	0.1U_0402_10V7K	HDMI TX2-
	24 VGA_HDMI_TXD2+	C235	DISO@	1	0.1U_0402_10V7K	HDMI TX2+
DIS	24 VGA_HDMI_TXD1-	C237	DISO@	1	0.1U_0402_10V7K	HDMI TX1-
	24 VGA_HDMI_TXD1+	C236	DISO@	1	0.1U_0402_10V7K	HDMI TX1+
DIS	24 VGA_HDMI_TXD0-	C241	DISO@	1	0.1U_0402_10V7K	HDMI TX0-
	24 VGA_HDMI_TXD0+	C240	DISO@	1	0.1U_0402_10V7K	HDMI TX0+
DIS	24 VGA_HDMI_TXC-	C239	DISO@	1	0.1U_0402_10V7K	HDMI CLK-
	24 VGA_HDMI_TXC+	C238	DISO@	1	0.1U_0402_10V7K	HDMI CLK+



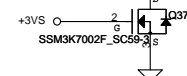
NVidia Recommend 05/10



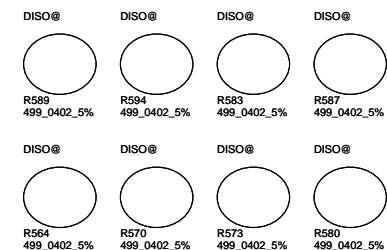
SM070001310 400ma 90ohm@100mhz DCR 0.3



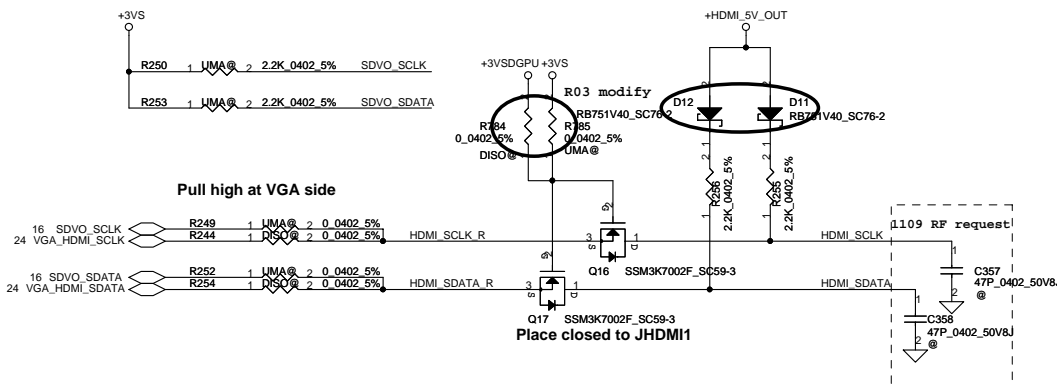
INTEL use 680 Ohm for terminationn in DG 1.5



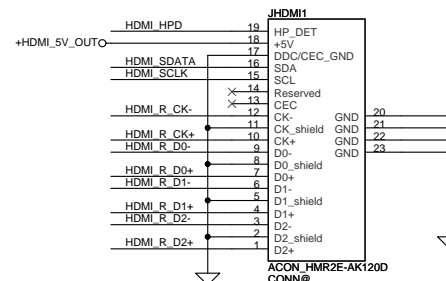
NV use 499 Ohm for terminationn



Pull high at VGA side



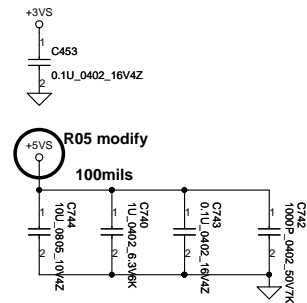
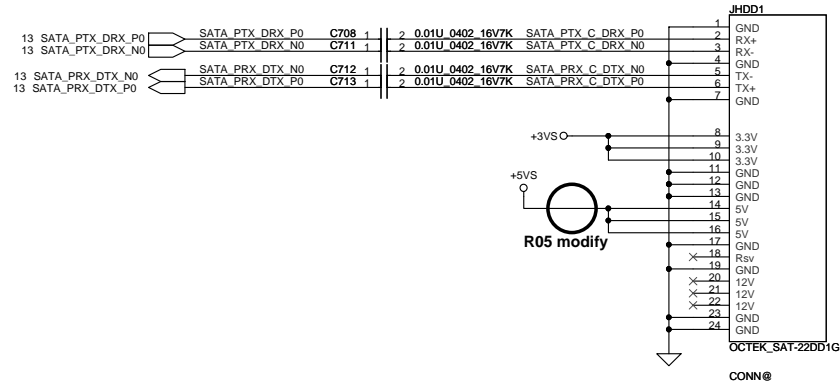
HDMI connector



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Issued Date	2011/02/08	Document Number	HDMI Conn
Deciphered Date	2012/02/08	Rev	JE50-HR/SJV50-HR M/B Schematics
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## SATA HDD1 Conn.

CL 4.0 mm



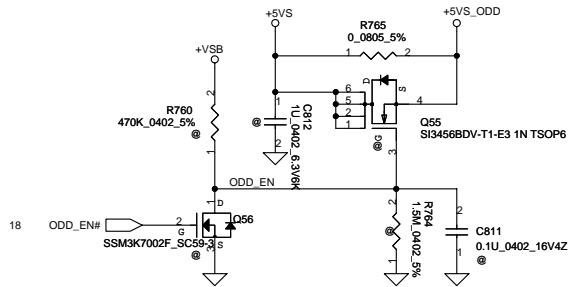
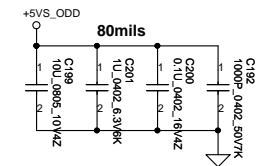
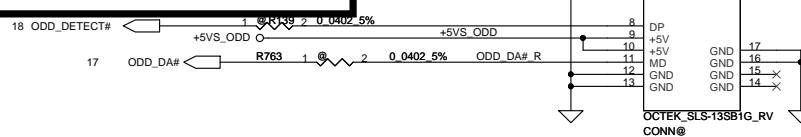
change to port1 cause by intel  
SATA II issue (20110201)

## SATA ODD Conn.

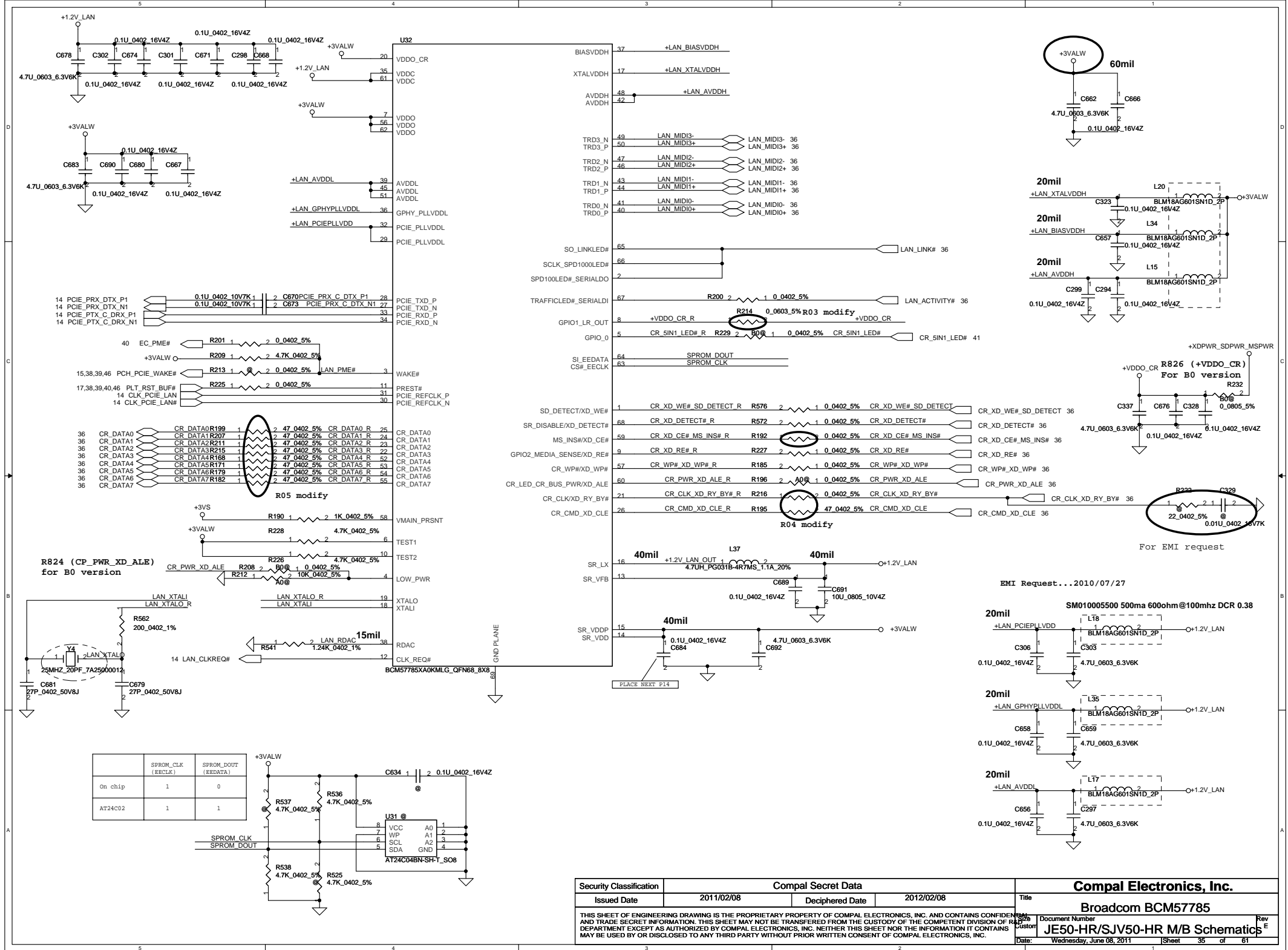
R20 modify

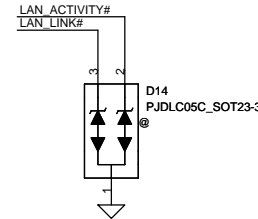
13 SATA\_PTX\_DRX\_P1  
13 SATA\_PTX\_DRX\_N1  
13 SATA\_PRX\_DTX\_N1  
13 SATA\_PRX\_DTX\_P1

C643 1 2 0.01U\_0402\_16V7K SATA\_PTX\_C\_DRX\_P2  
C639 1 2 0.01U\_0402\_16V7K SATA\_PTX\_C\_DRX\_N2  
C628 1 2 0.01U\_0402\_16V7K SATA\_PRX\_C\_DTX\_N2  
C624 1 2 0.01U\_0402\_16V7K SATA\_PRX\_C\_DTX\_P2



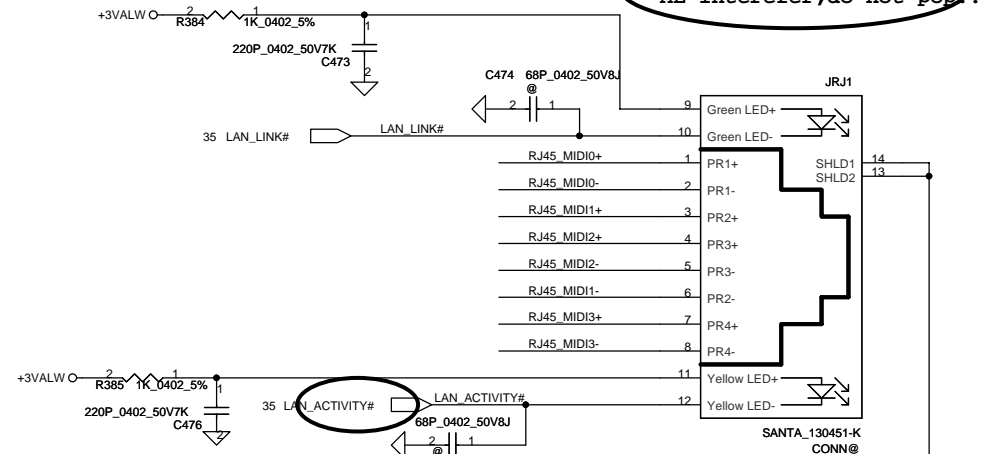
Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2011/02/08		Deciphered Date		2012/02/08		Title					
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								Document Number		JE50-HR/SJV50-HR M/B Schematics		Rev E	
								Date: Wednesday, June 08, 2011		Sheet 34 of 61			



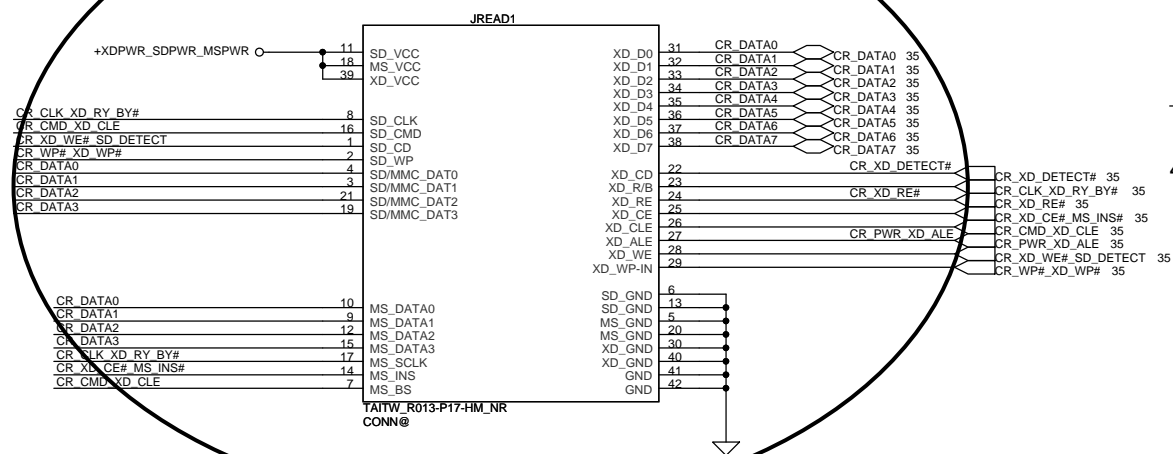


## R03 modify

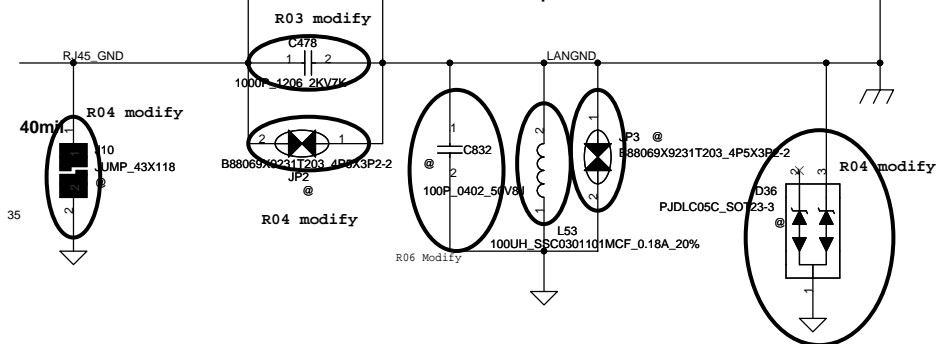
C474,C475 and D14  
ME interfere,do not pop!!



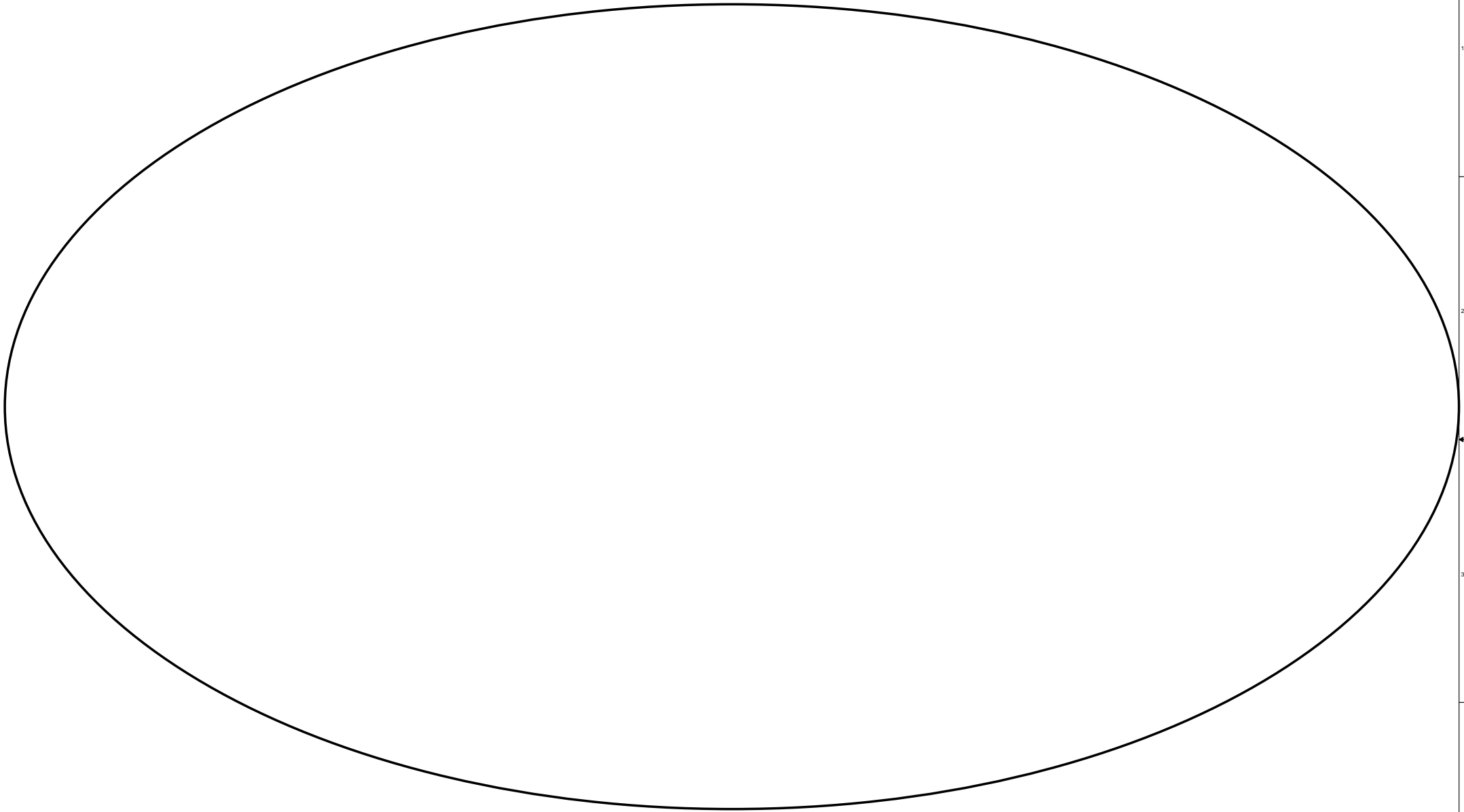
R05 modify



## EMI Request

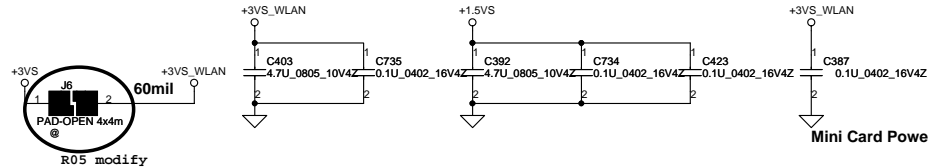


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Issued Date	2011/02/08	Deciphered Date	2012/02/08	Title	LAN Magnetic & RJ45	
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				Custom	JE50-HR/SJV50-HR M/B Schematics	E
				Date:	Wednesday, June 08, 2011	Sheet 36 of 61

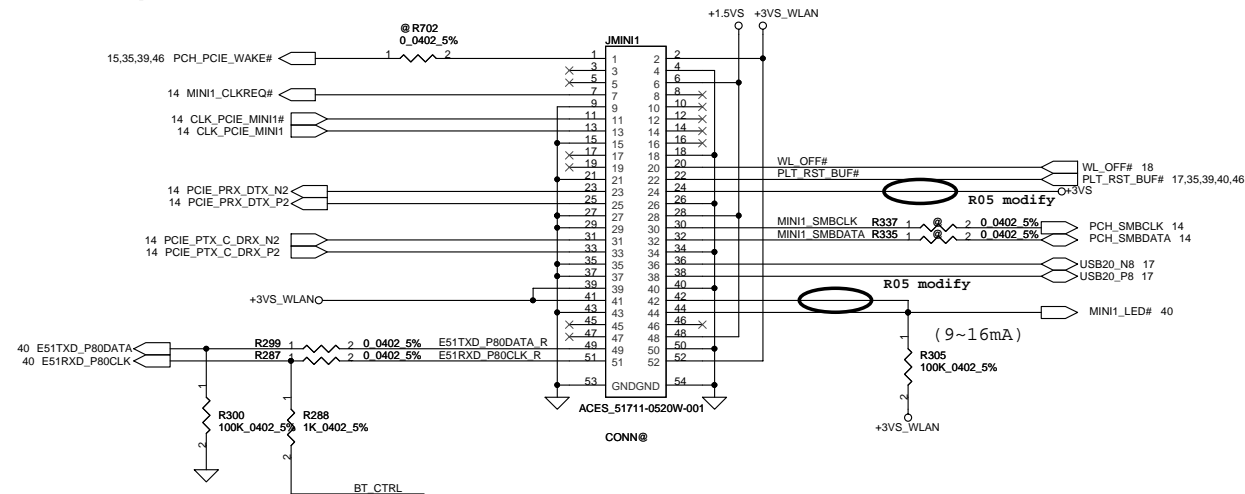


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				Date:	Wednesday, June 08, 2011
				Sheet	37 of 61

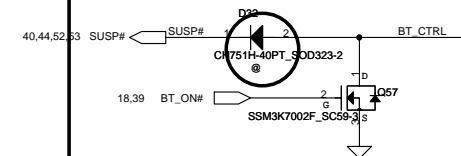
Figure 1: Schematic diagram of the power supply circuit for the Mini Card Power module. The diagram shows four stages of power regulation. Stage 1: A 3VS input is connected to a 60mil trace, which then goes through a 4.7uF capacitor (C403) and a 0.1uF capacitor (C735) to a 3VS\_WLAN output. Stage 2: A 1.5VS input is connected to a 4.7uF capacitor (C392) and a 0.1uF capacitor (C734) to a 3VS\_WLAN output. Stage 3: A 3VS\_WLAN input is connected to a 4.7uF capacitor (C423) and a 0.1uF capacitor (C387) to a 3VS\_WLAN output. Stage 4: A 3VS\_WLAN input is connected to a 4.7uF capacitor (C423) and a 0.1uF capacitor (C387) to a 3VS\_WLAN output. The diagram also includes a note 'R05 modify' and a 'PAD-OPEN 4x4mm' label.



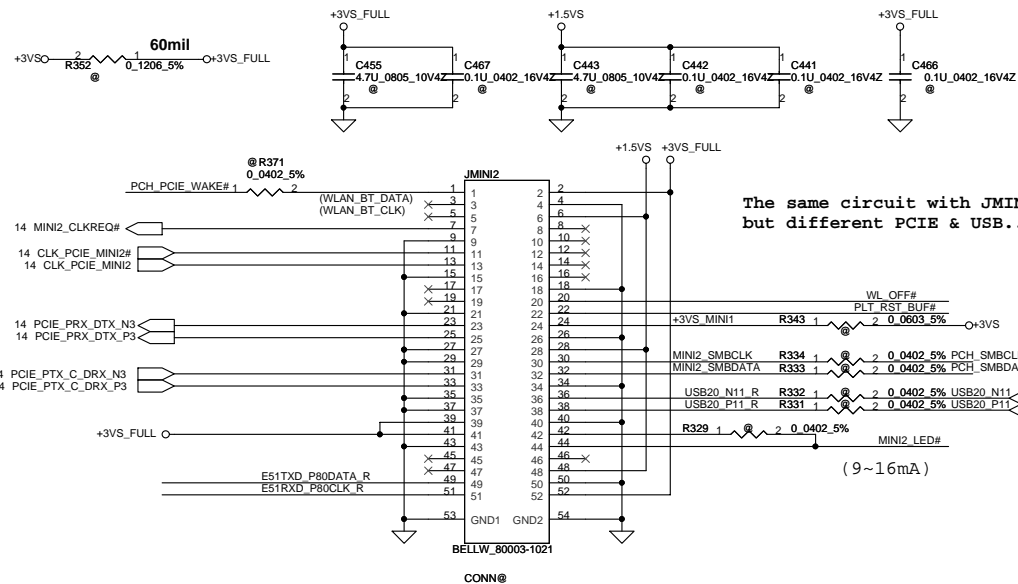
### Mini Card Power Rating



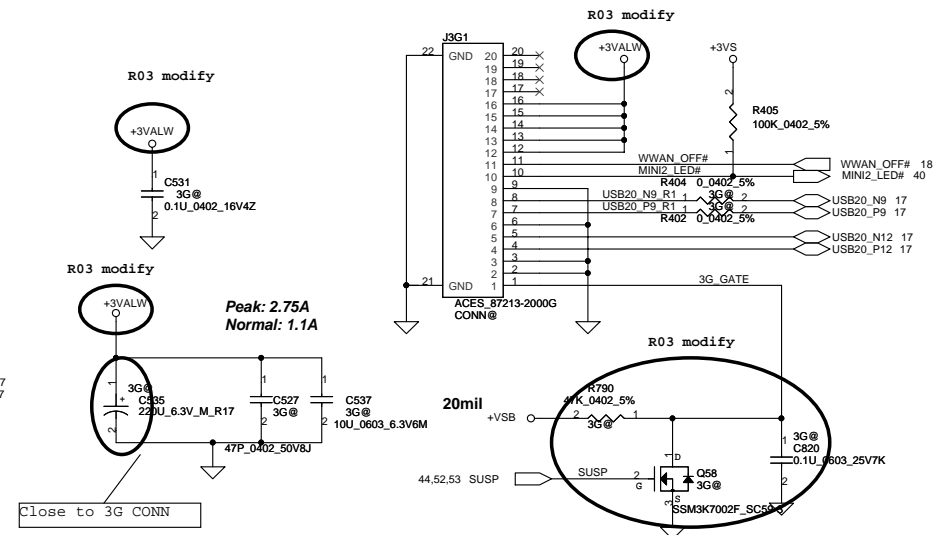
	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

[illegible]

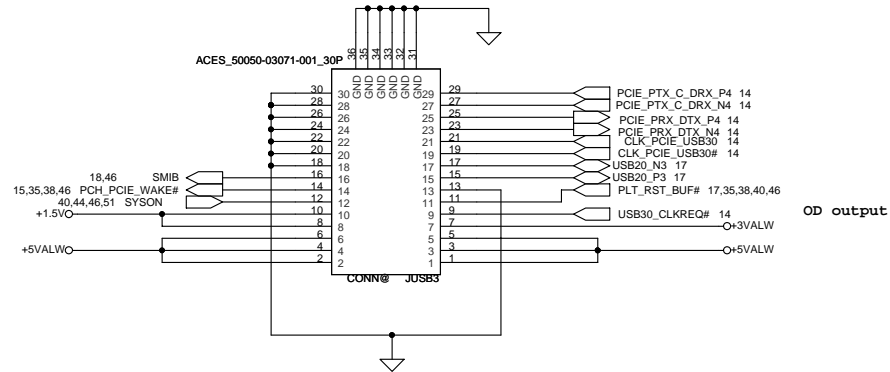
The same circuit with JMINI1,  
but different PCIE & USB....



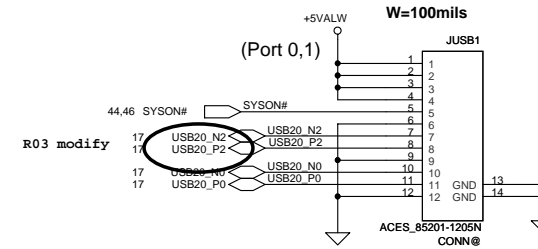
### To 3G Module Connect



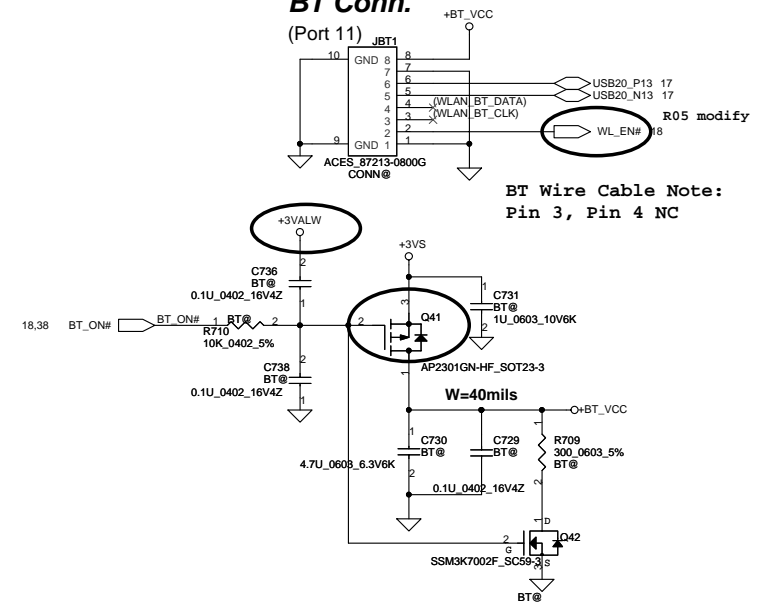
**USB3.0 Conn.**



## USB/B Conn.



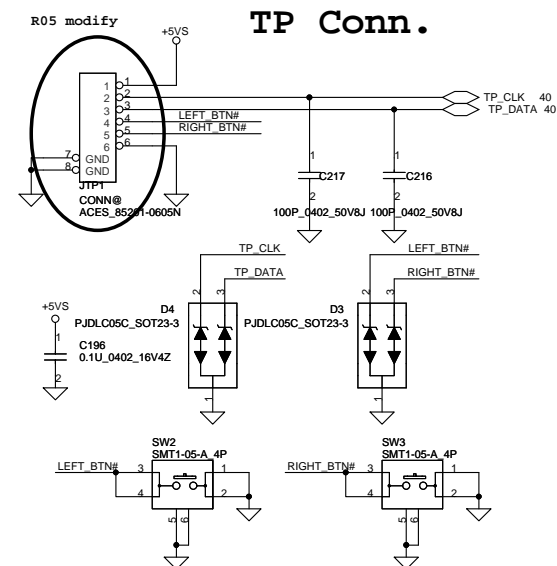
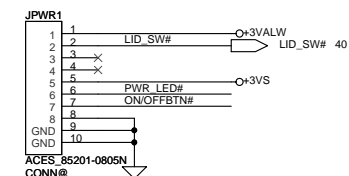
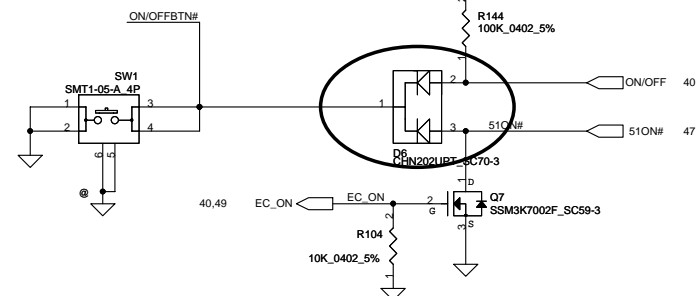
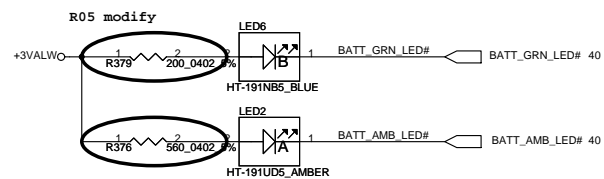
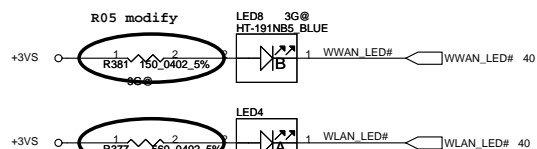
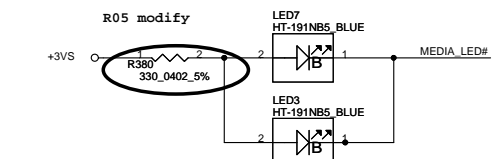
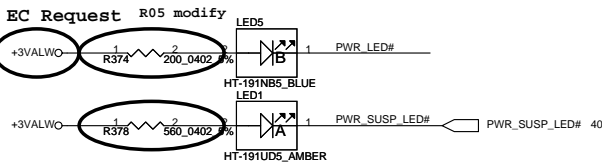
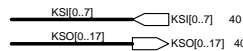
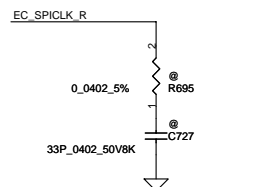
***BT Conn.***



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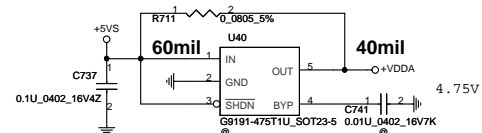




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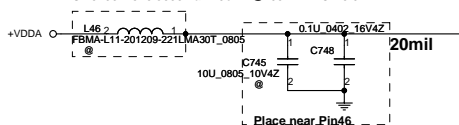
Document Number  
JE50-HR/SJV50-HR M/B Schematics

Rev E



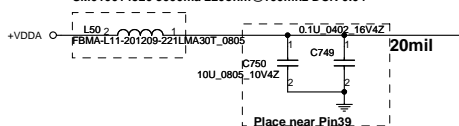
(output = 300 mA)

SM010014520 3000ma 220ohm@100mhz DCR 0.04



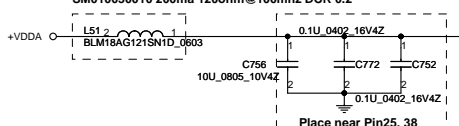
Place near Pin46

SM010014520 3000ma 220ohm@100mhz DCR 0.04

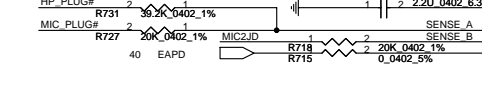
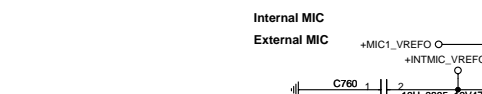
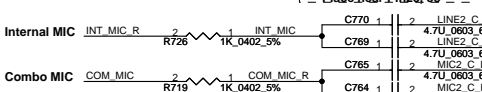


Place near Pin39

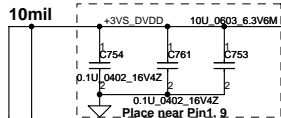
SM010030010 200ma 120ohm@100mhz DCR 0.2



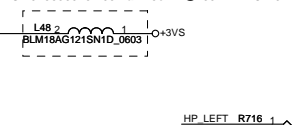
Place near Pin25, 38



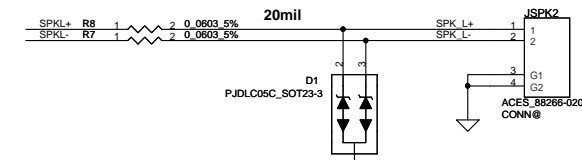
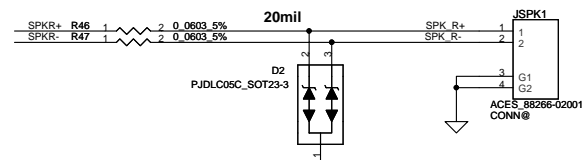
## HD Audio Codec



SM010030010 200ma 120ohm@100mhz DCR 0.2

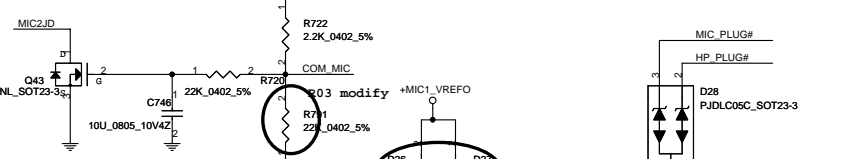
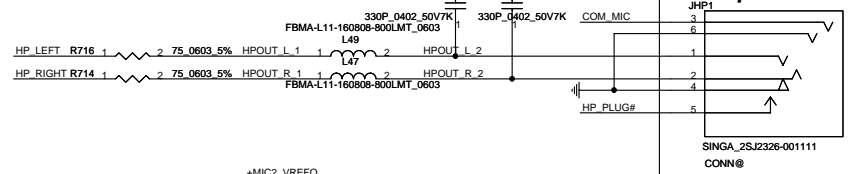


## Int. Speaker Conn.

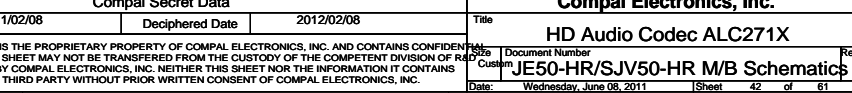
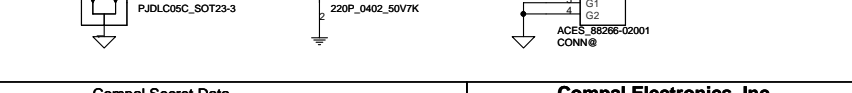
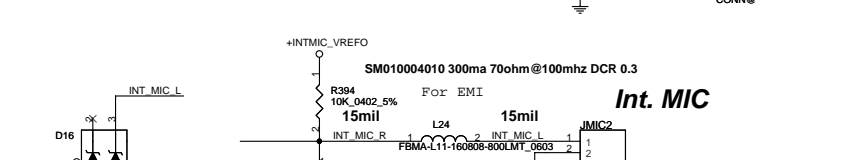
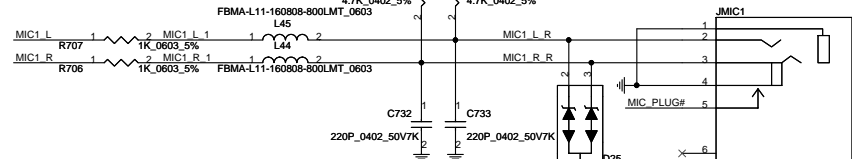


Singatron 2SJ2326  
DC021007151

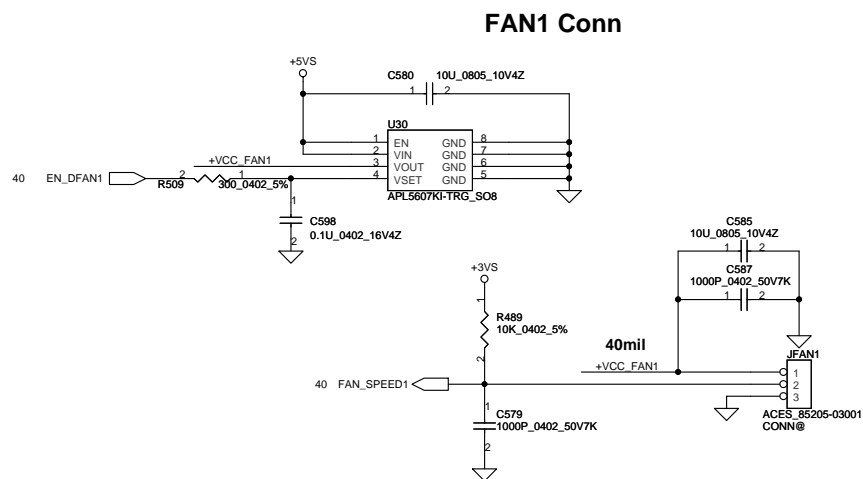
## Headphone Out



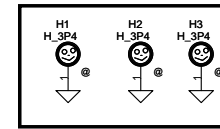
## MIC JACK



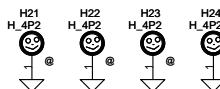
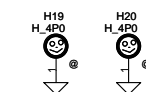
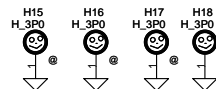
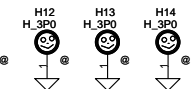
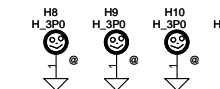
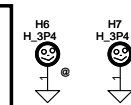
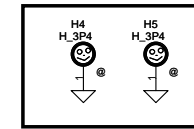
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Issued Date				2011/02/08				Deciphered Date			
2012/02/08				Title				HD Audio Codec ALC271X			
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### FAN Stand-Off

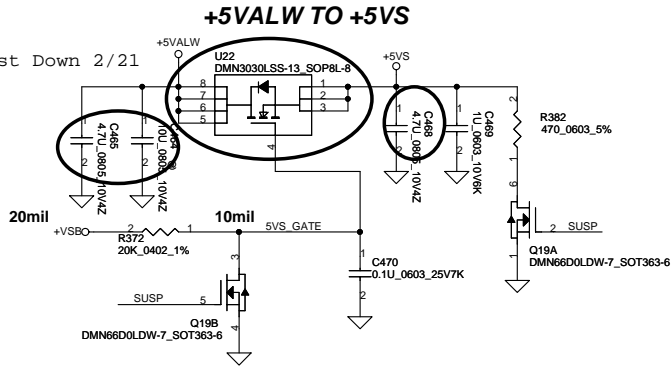


### JUSB3 Stand-Off

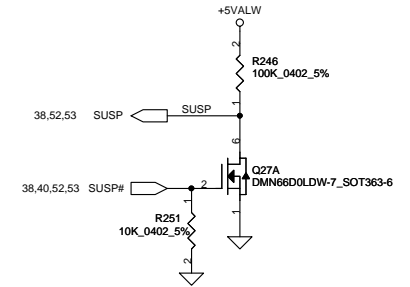
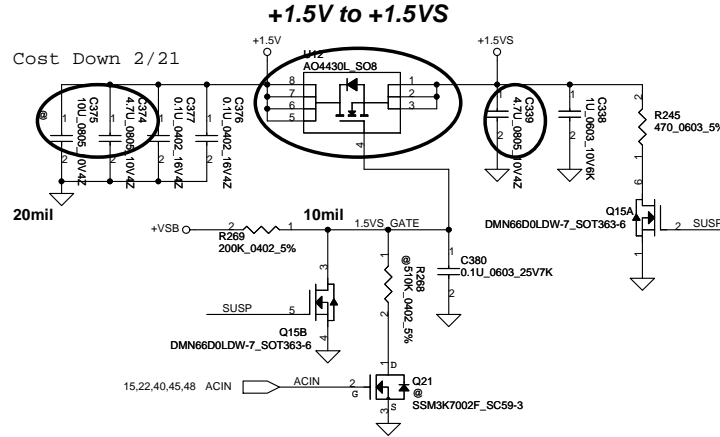


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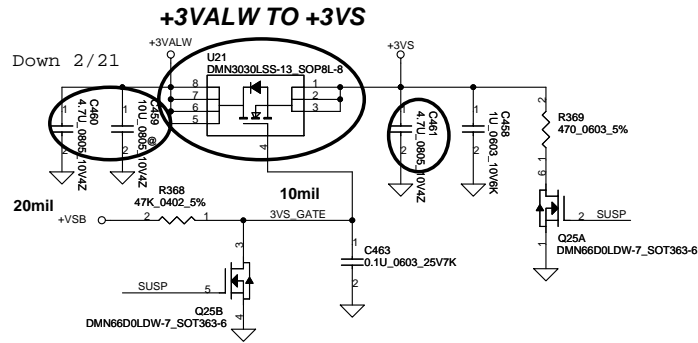
For Cost Down 2/21



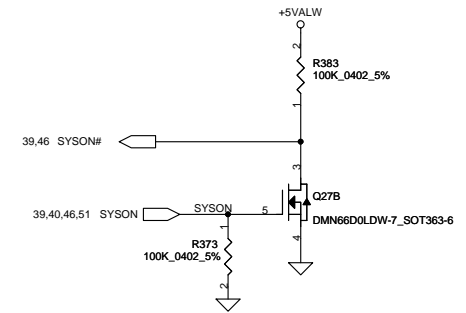
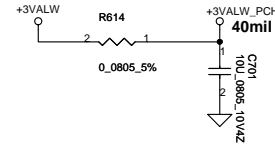
For Cost Down 2/21



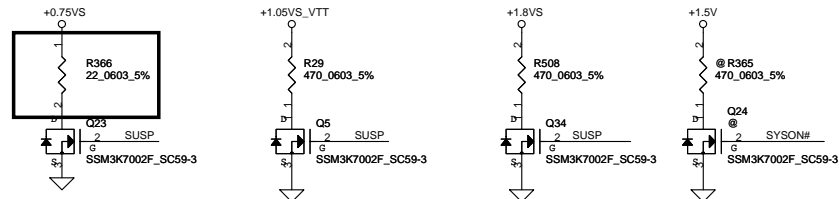
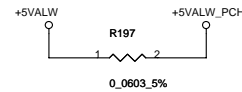
For Cost Down 2/21



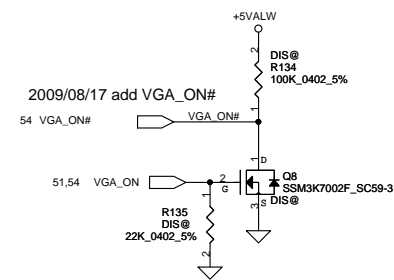
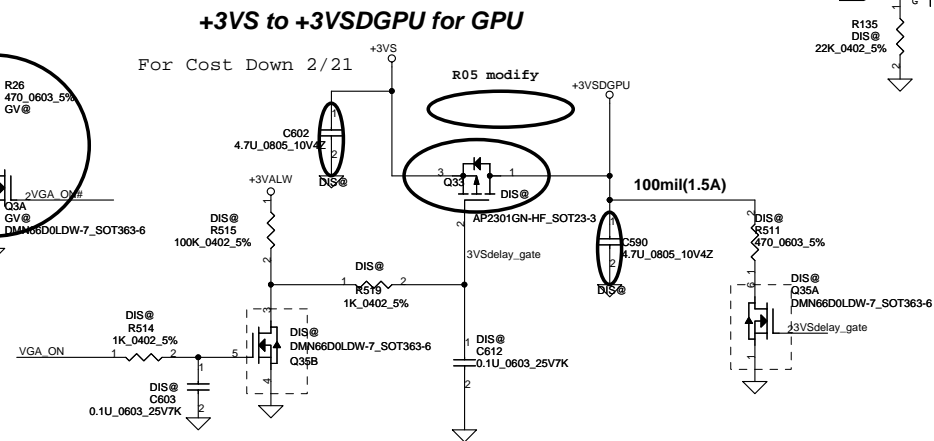
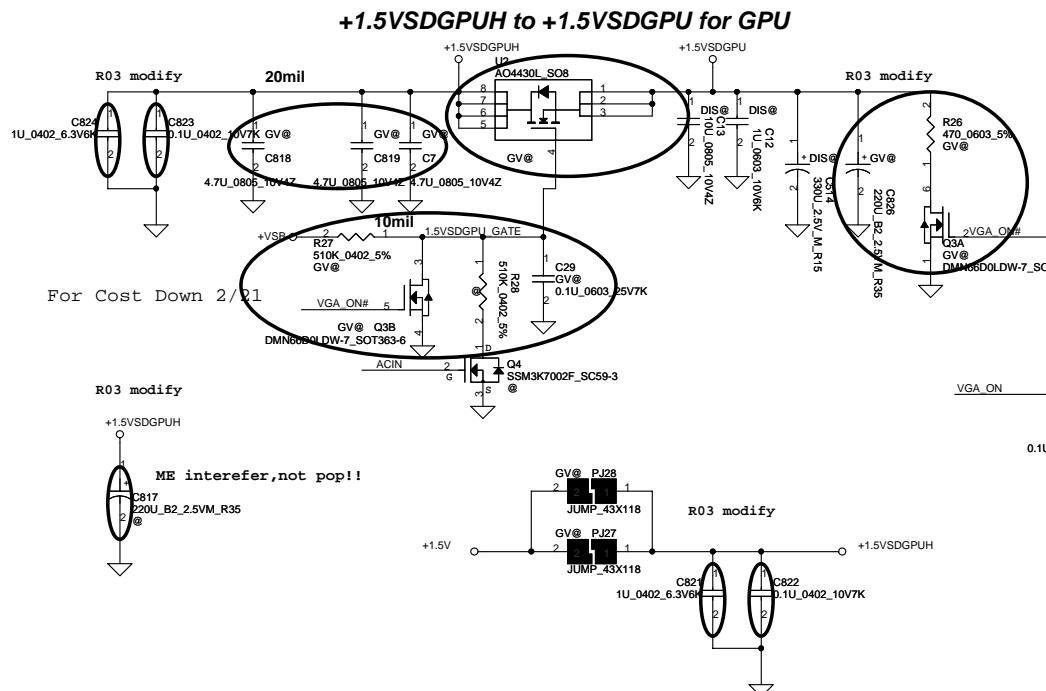
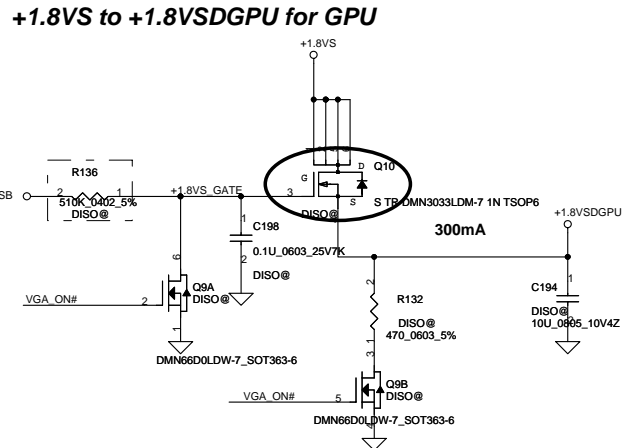
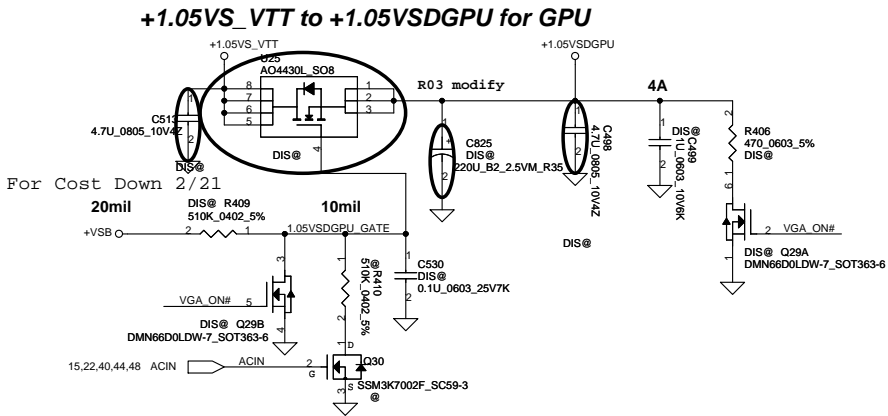
**+3VALW TO +3VALW\_PCH(PCH AUX Power)**



**+5VALW TO +5VALW\_PCH(PCH AUX Power)**

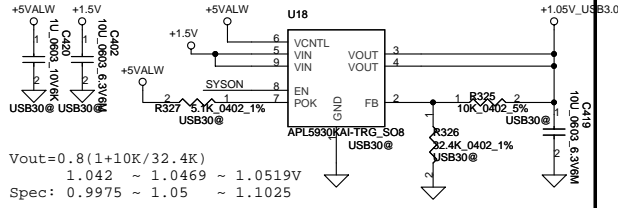


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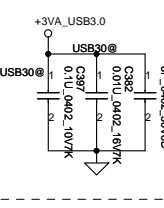


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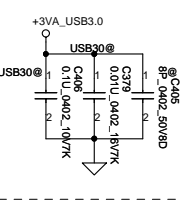
# +1.5V to +1.05V Transfer



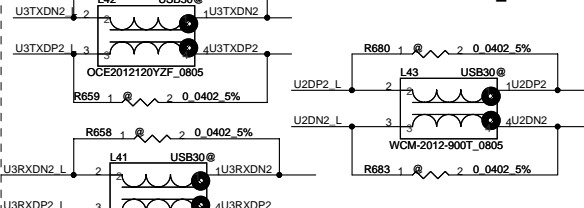
# Close to U3.D7



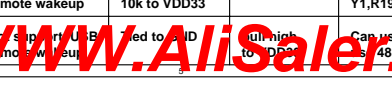
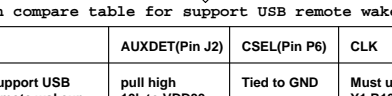
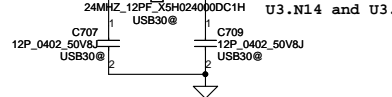
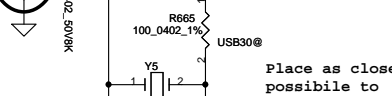
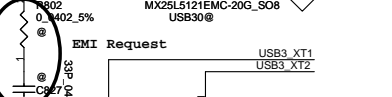
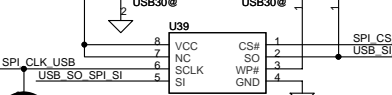
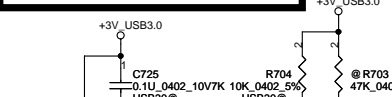
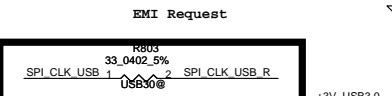
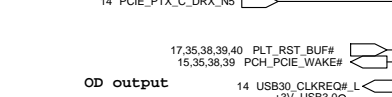
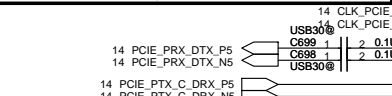
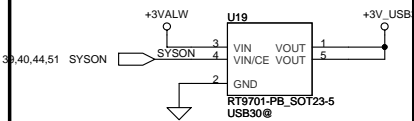
# Close to U3.P13



# For EMI request



# +3VALW to +3V Transfer



SPEC Max: +3V---200mA; +1.05V---800mA

Idle mode: 0.489W:

+3V---43mA; +1.05V---328mA

D3 mode: 0.066W:

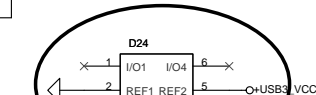
+3V---5.4mA; +1.05V---45mA

Can be attach to EC, either.

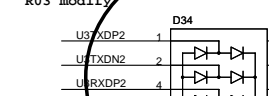
PCI Express/ExpressCard select signal  
1: others  
2: Express Card or Mini card

As short as possible

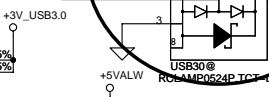
For USB2.0 ESD request



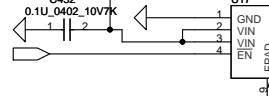
For ESD request



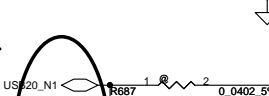
R03 modify



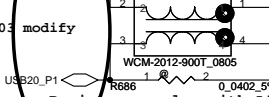
W=60mils



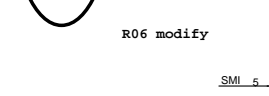
R03 modify



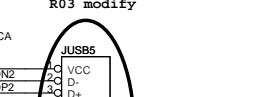
Resistor overlap with L52



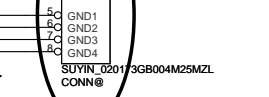
R06 modify



R03 modify



USB2.0 Conn



PN: SP060004B00

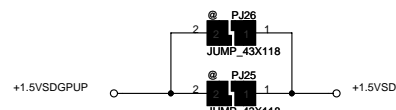
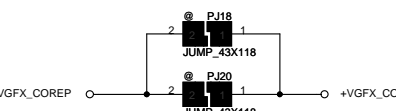
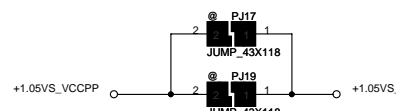
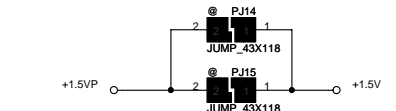
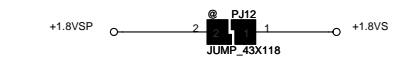
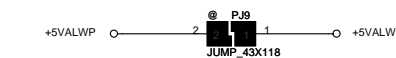
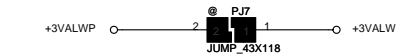
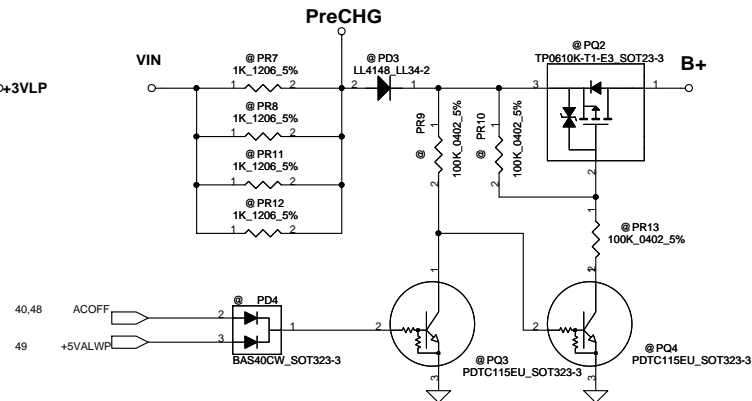
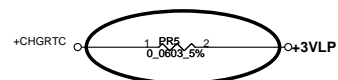
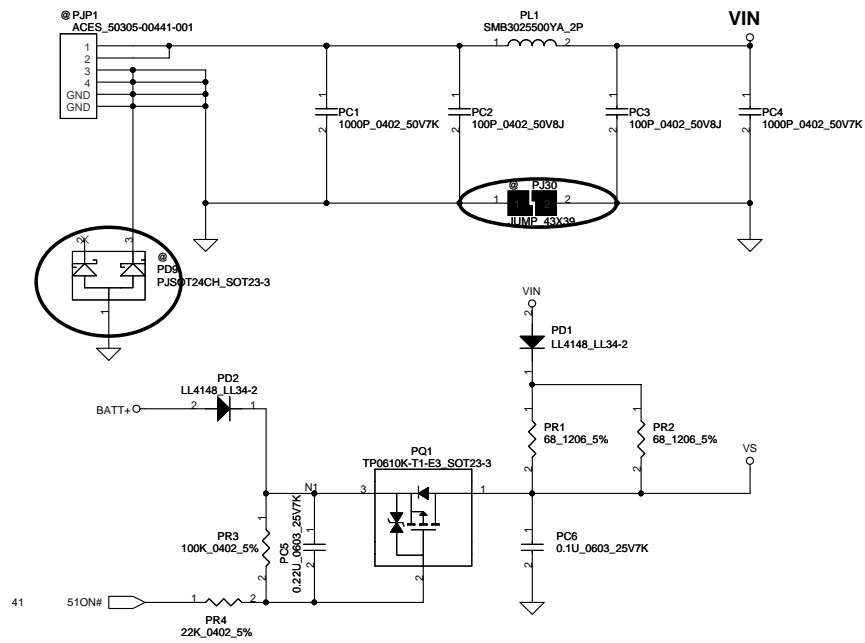
Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41

Can use either 18MHz or 24MHz When 48MHz clock mode. R22, R25

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Title	USB3.0 PD720200		
Document Number			
Rev E			
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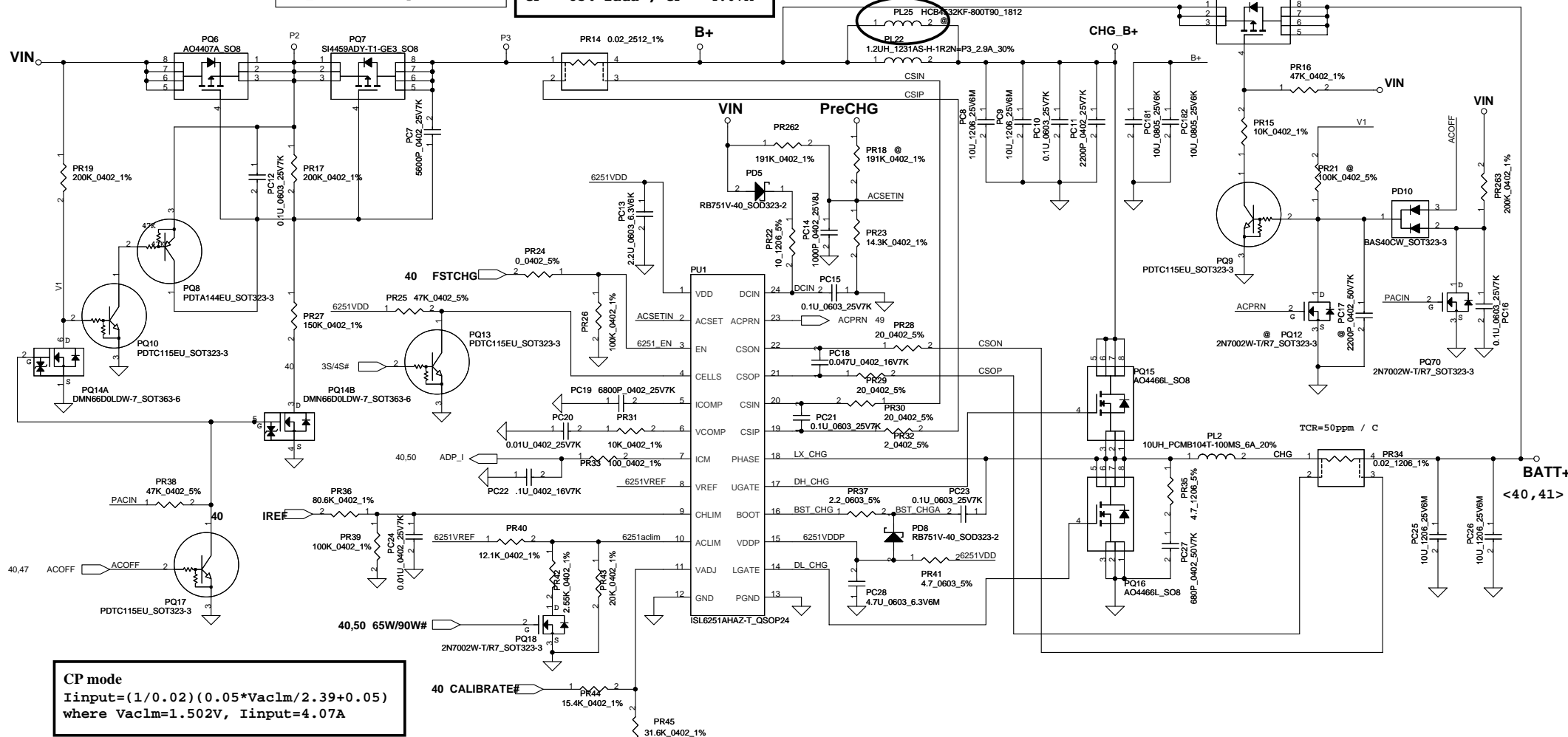
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				Rev
				Custom
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Iada=0~4.74A(90W/19V=4.736A)

ADP\_I = 19.9\*Iadapter\*Rsense

CP = 85%\*Iada ; CP = 4.07A

PC181 and PC182 reserve for EMI Isen solution



**CP mode**  
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$   
 where  $V_{ac1m} = 1.502V$ ,  $I_{input} = 4.07A$

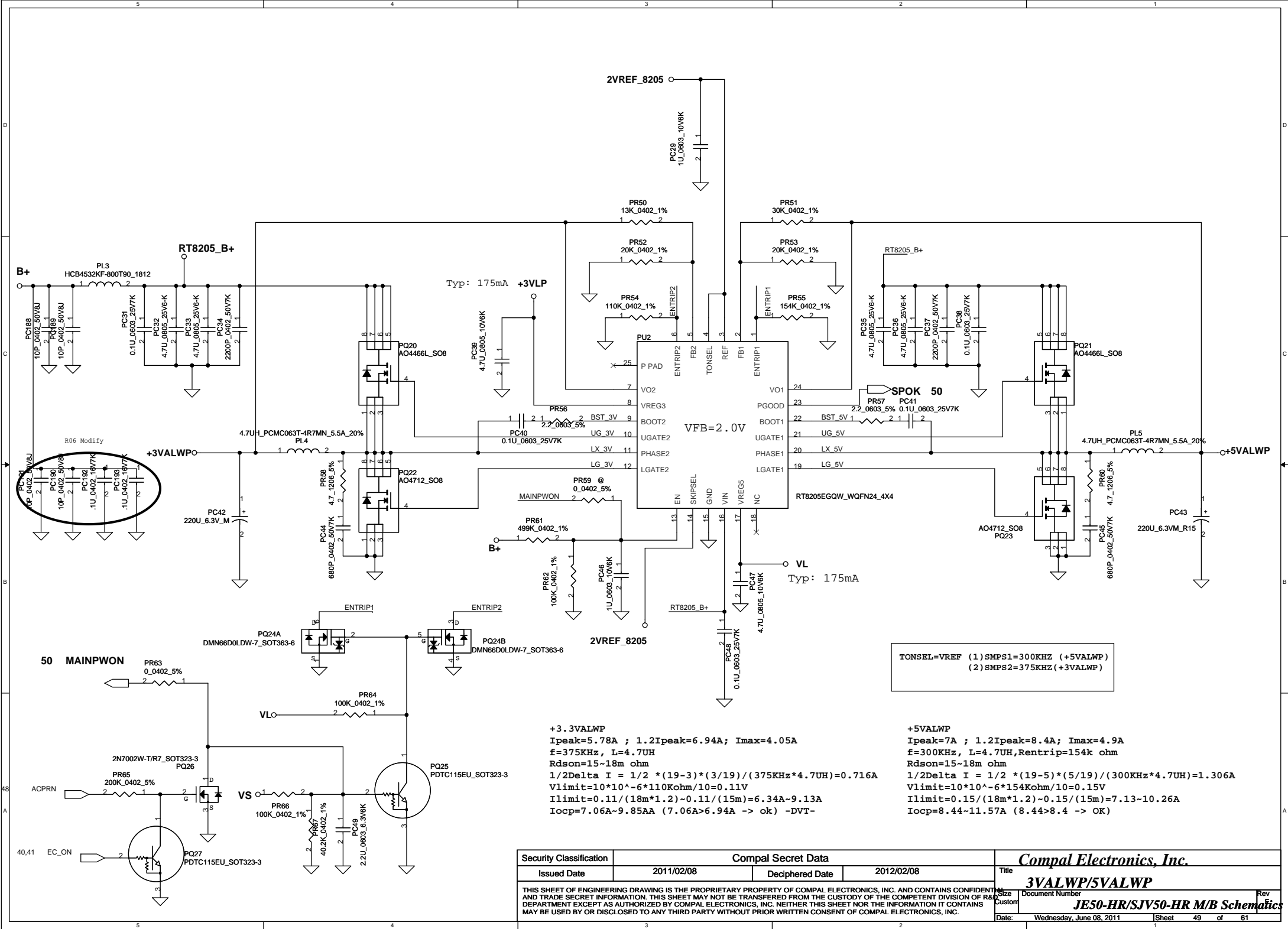
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A
$I_{REF} = 0.7224 * I_{charge}$
$I_{REF} = 0.43V \sim 3.24V$

Ki  
 $V_{chlim} = I_{ref} * (PR374 / (PR372 + PR374))$   
 $= I_{ref} * (100K / (80.6K + 100K))$   
 $= I_{ref} * 0.5537$   
 $I_{charge} = (165mV / PR369) * (V_{chlim} / 3.3V)$   
 $= (165m / 20m) * (1 / 3.3V) * I_{ref} * 0.5537$   
 $= 1.3842 * I_{ref}$   
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow Ki = 0.7224$

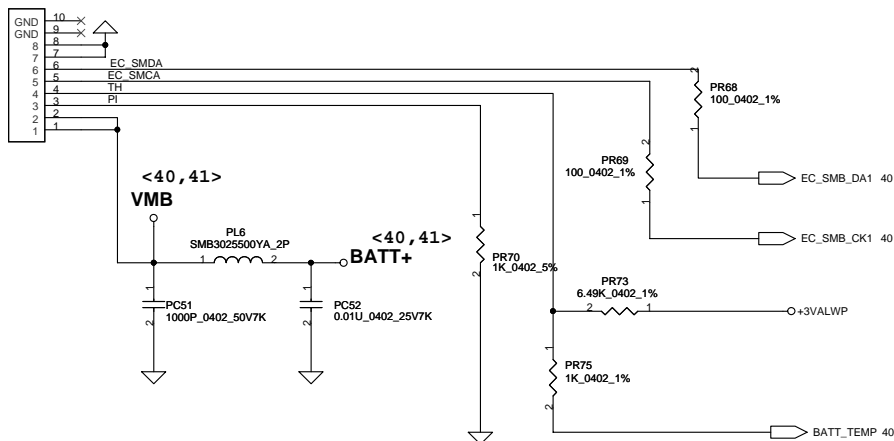
Kv  
 $R_{internal} = 514K$   $R_{ec} = 3K$   $R_1 = PR379 = 15.4K$   $R_2 = PR381 = 31.6K$   
 $R = 514K / (31.6K / (15.4K + 3K) + 1) = 11.372K$   
 $r = 514K / (514K / 31.6K + 1) = 28.14K$   
 $V_{cell} = 0.175 * V_{adj} + 3.99V$   
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$   
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$   
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$   
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * Kv = (4.2 - (4.2 + A * 0.175)) * Kv$   
 $A = V_{ref} * (R / (R + 514K)) = 0.052$



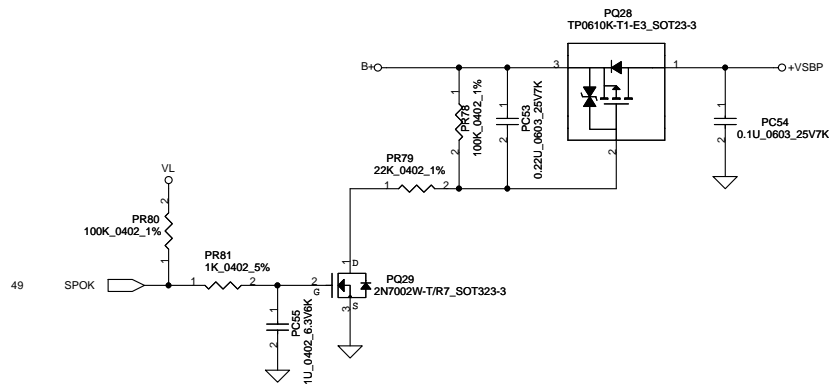
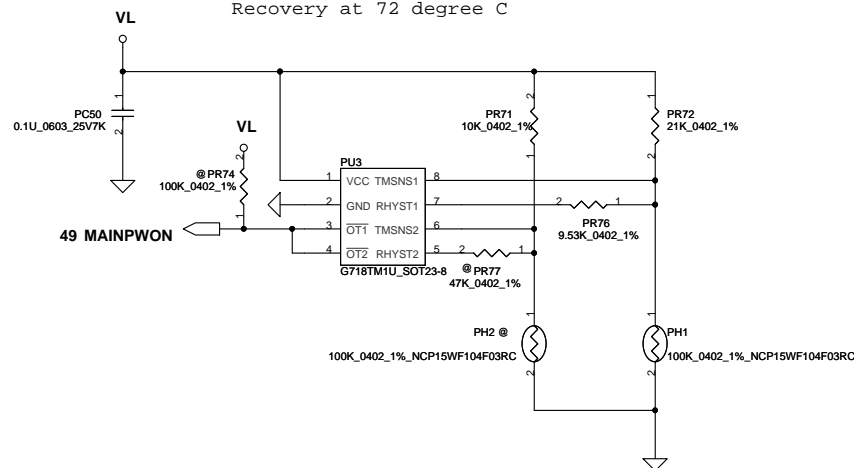


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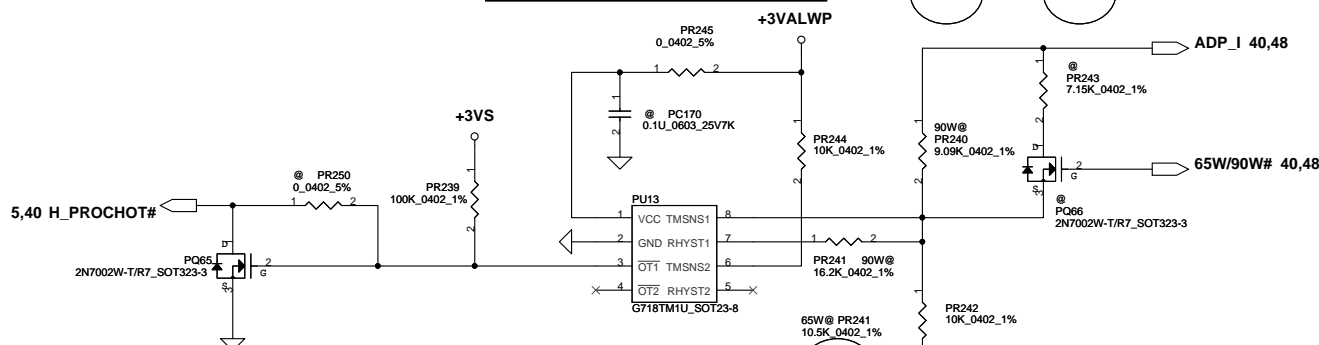
PJP2  
SUYIN\_200275GR008G13GZR



PH1 under CPU botten side :  
CPU thermal protection at 92 degree C  
Recovery at 72 degree C



Change 5VALW to 3VALW on DVT



For 65W adapter==>action 70W , Recovery 54W  
For 90W adapter==>action 97W , Recovery 75W  
For 120W adapter==>action 135W , Recovery 100W

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39,40,44,46 SYSON

+5VALW

<Vo=1.5V> VFB=0.75V  
V=0.75\*(1+10K/10K)=1.5V  
Fsw=298KHz

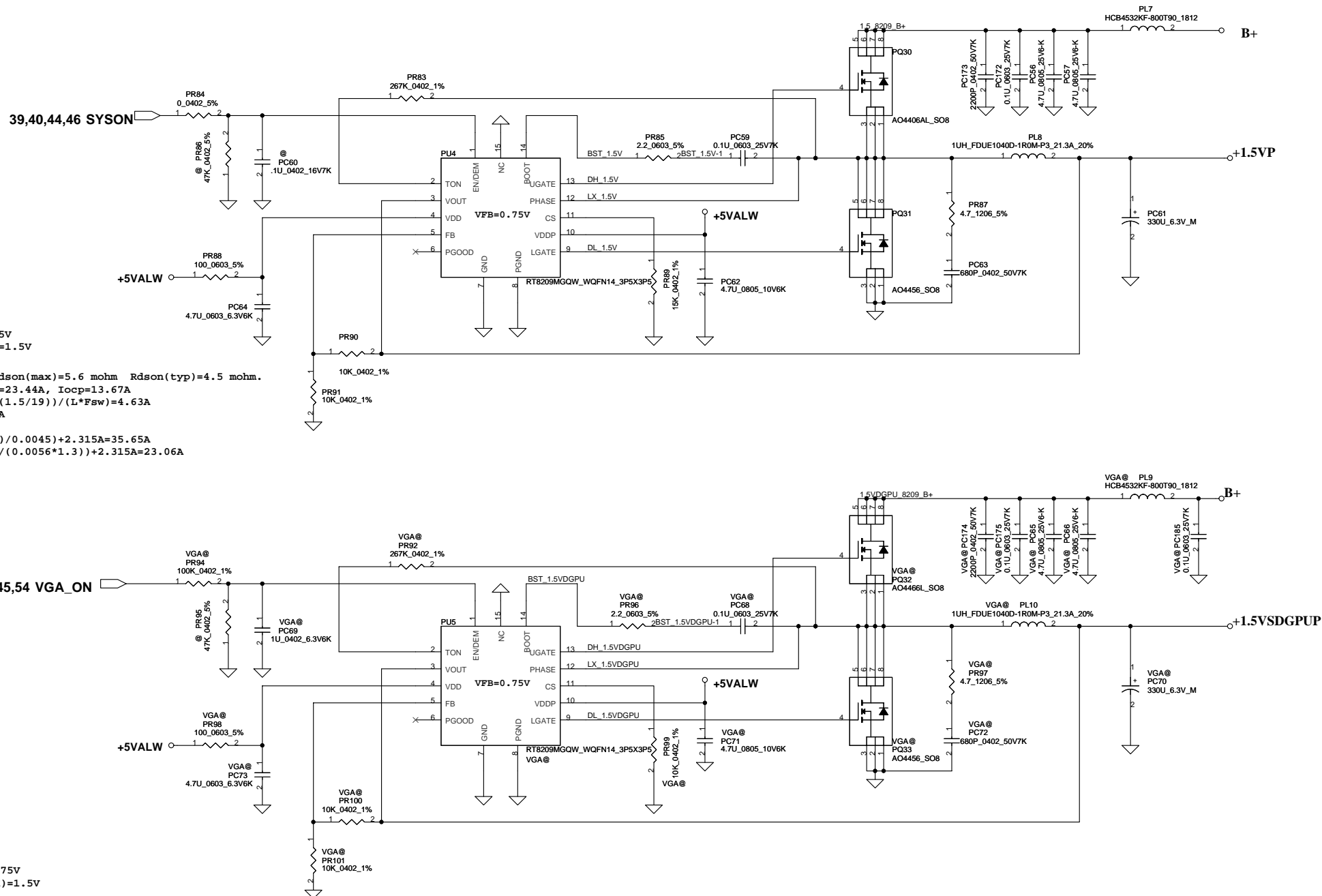
Cout ESR=15m ohm Rds(on)(max)=5.6 mohm Rds(on)(typ)=4.5 mohm.  
Ipeak=19.53A, Imax=23.44A, Iocp=13.67A  
Delta I=((19-1.5)\*(1.5/19))/(L\*Fsw)=4.63A  
=>1/2Delta I=2.315A  
choose Rcs=15K  
Iocpmax=((15K\*11uA)/(0.0045))+2.315A=35.65A  
Iocpmin=((15K\*9uA)/(0.0056\*1.3))+2.315A=23.06A  
Iocp=23.06A~35.65A

45,54 VGA\_ON

+5VALW

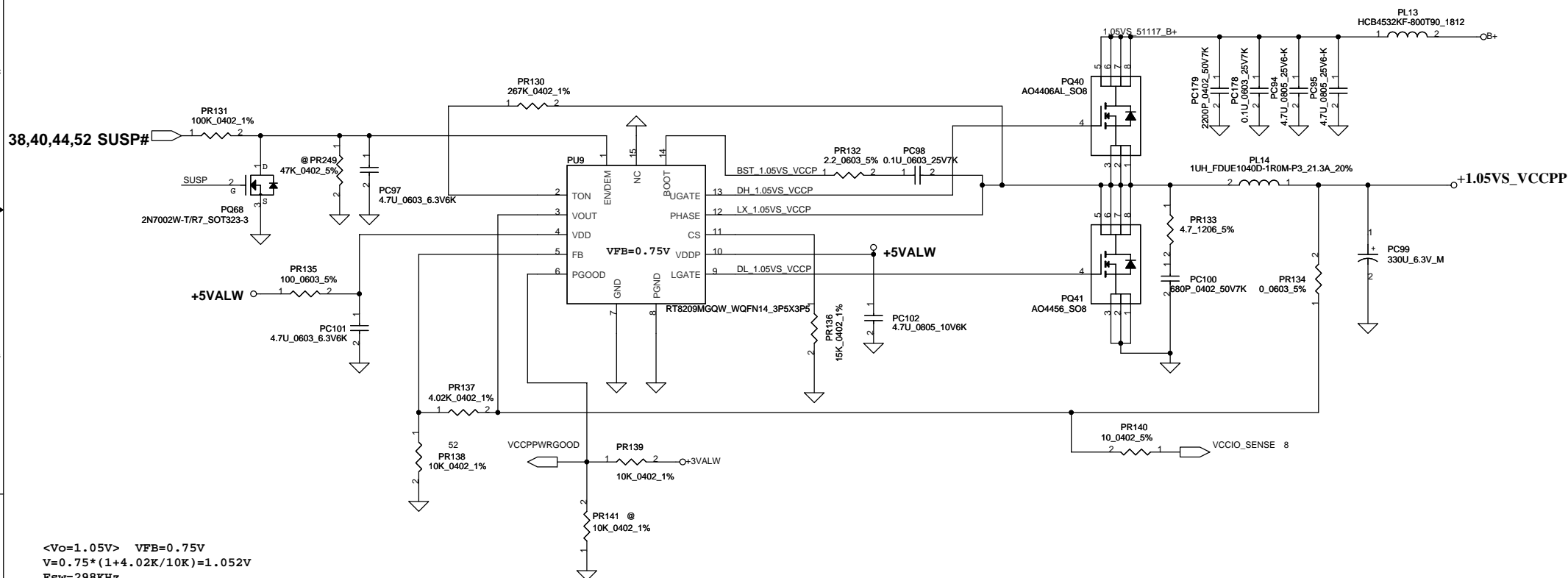
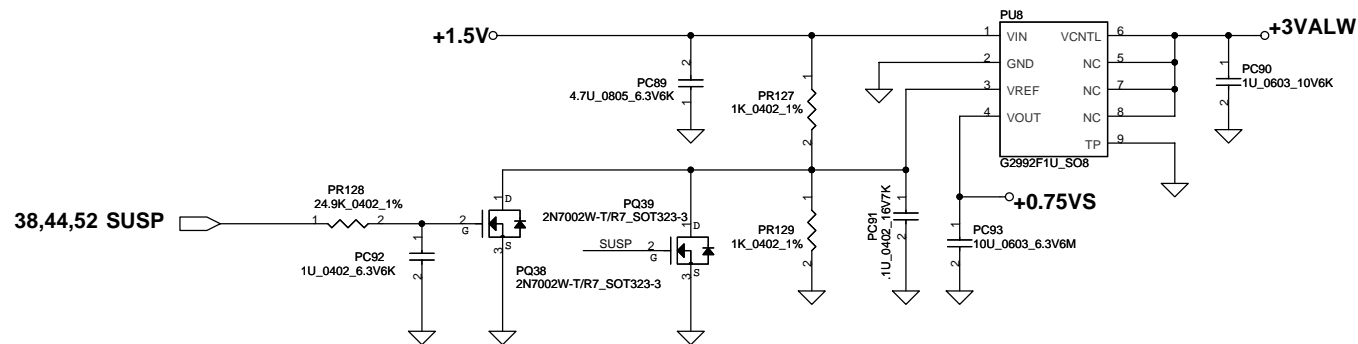
<Vo=1.5V> VFB=0.75V  
V=0.75\*(1+10K/10K)=1.5V  
Fsw=298KHz

Cout ESR=15m ohm Rds(on)(max)=5.6 mohm Rds(on)(typ)=4.5 mohm.  
Ipeak=10.4A, Imax=12.48A, Iocp=7.28A  
Delta I=((19-1.5)\*(1.5/19))/(L\*Fsw)=4.63A  
=>1/2Delta I=2.315A  
choose Rcs=10K  
Iocpmax=((10K\*11uA)/(0.0045))+2.315A=24.59A  
Iocpmin=((10K\*9uA)/(0.0056\*1.3))+2.315A=15.95A  
Iocp=15.95A~24.59A



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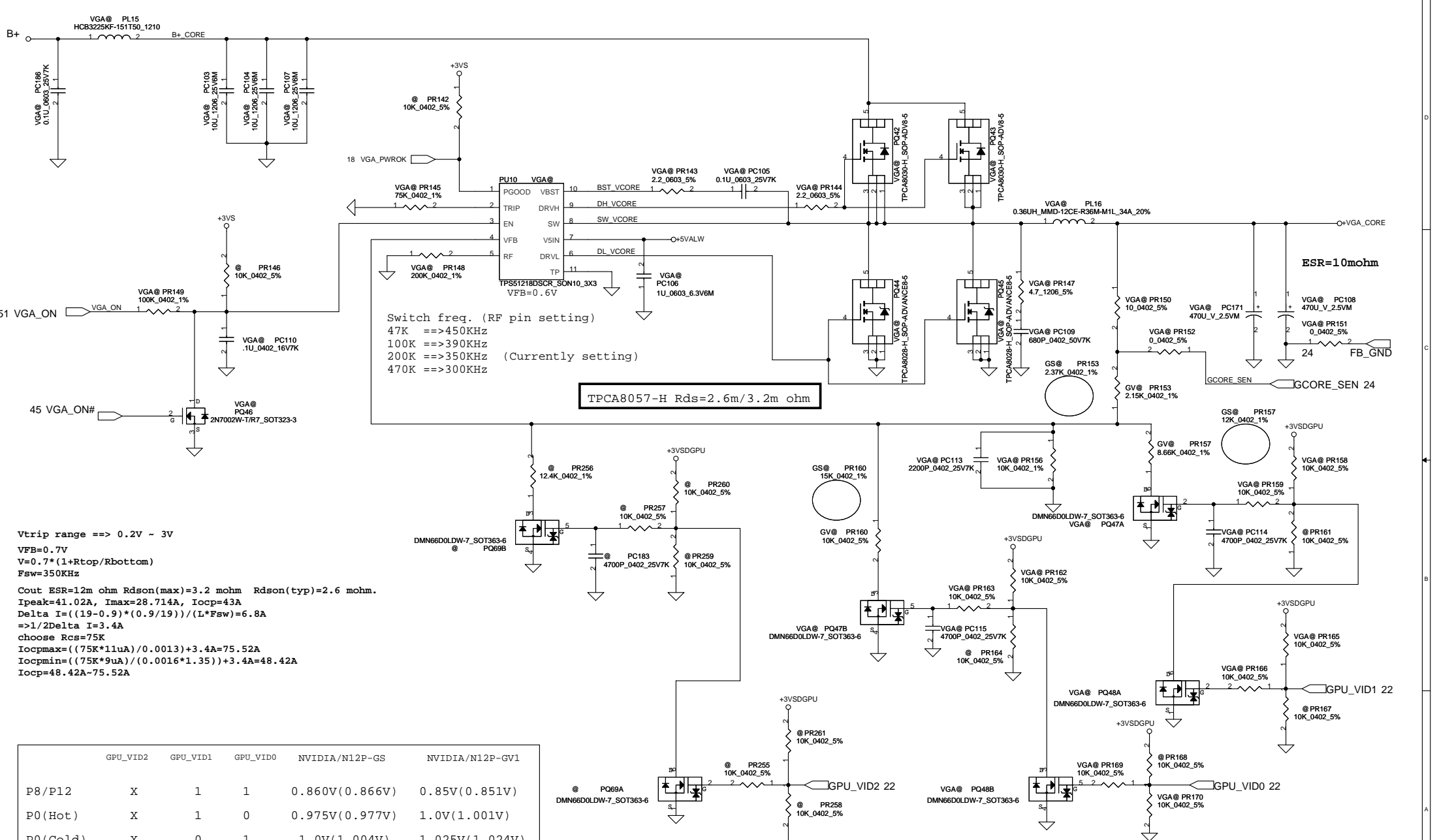




<Vo=1.05V> VFB=0.75V  
 $V=0.75 \times (1 + 4.02K/10K) = 1.052V$   
 $F_{sw} = 298KHz$

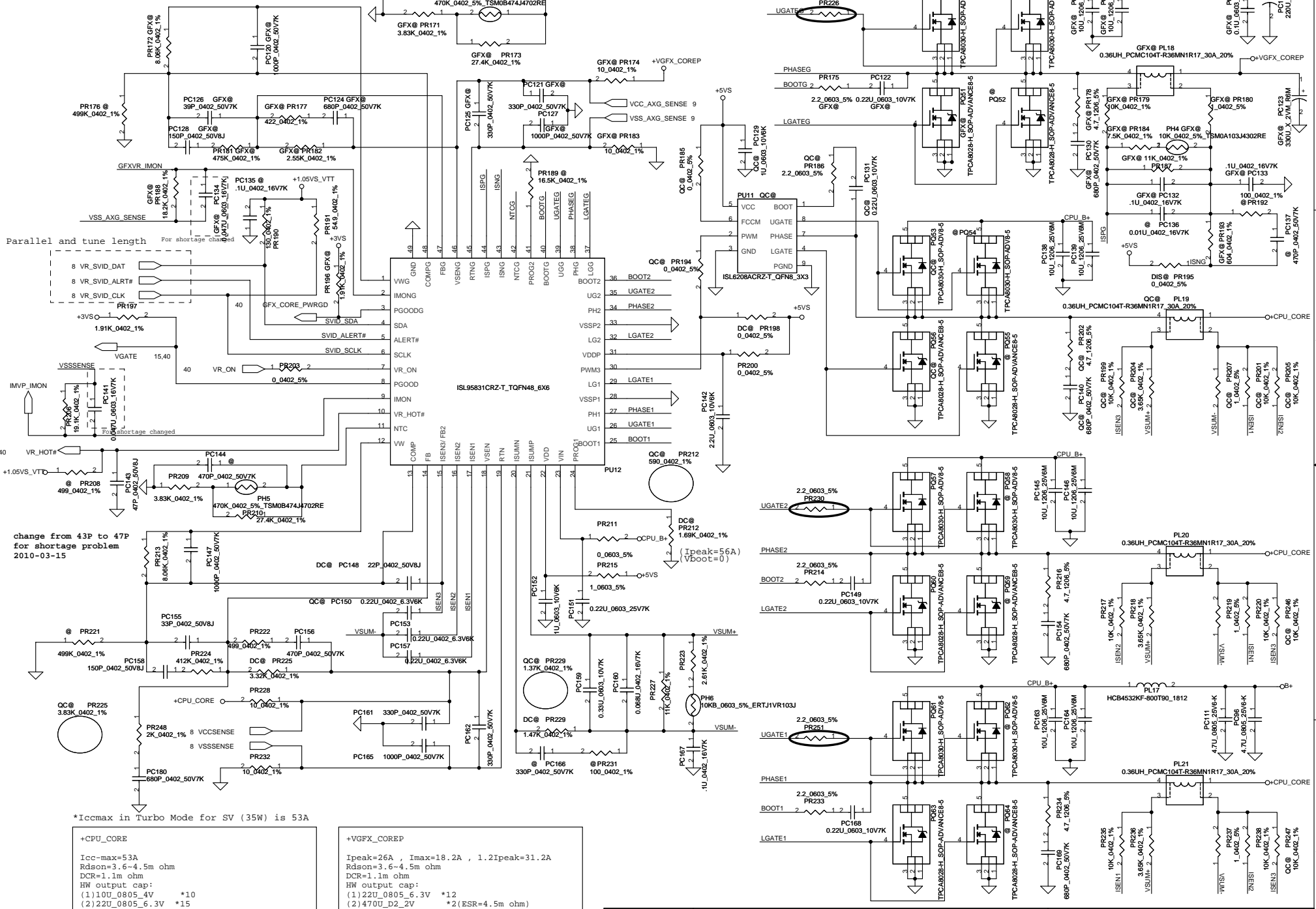
$C_{out} ESR = 15m \text{ ohm}$   $R_{dson(max)} = 5.6 \text{ mohm}$   $R_{dson(typ)} = 4.5 \text{ mohm}$ .  
 $I_{peak} = 12.866A$ ,  $I_{max} = 9A$ ,  $I_{ocp} = 15.439A$   
 $\Delta I = ((19 - 1.05) \times (1.05/19)) / (L \times F_{sw}) = 3.33A$   
 $\Rightarrow 1/2 \Delta I = 1.665A$   
choose  $R_{cs} = 15K$   
 $I_{ocpmax} = ((15K \times 11uA) / 0.0045) + 1.665A = 37.62A$   
 $I_{ocpmin} = ((15K \times 9uA) / (0.0056 \times 1.3)) + 1.665A = 23.02A$   
 $I_{ocp} = 23.02A \sim 37.62A$

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						Size		Document Number		P5WE0		Rev	
						Date:		Wednesday, June 08, 2011		Sheet		54 of 61	
3		1		2		1							

Alert# PU resistor need close CPU,  
so the PU resistor in HW schematic.  
but DAT and CLK need close PWM-IC,  
so the PU resistor in POWER schematic.



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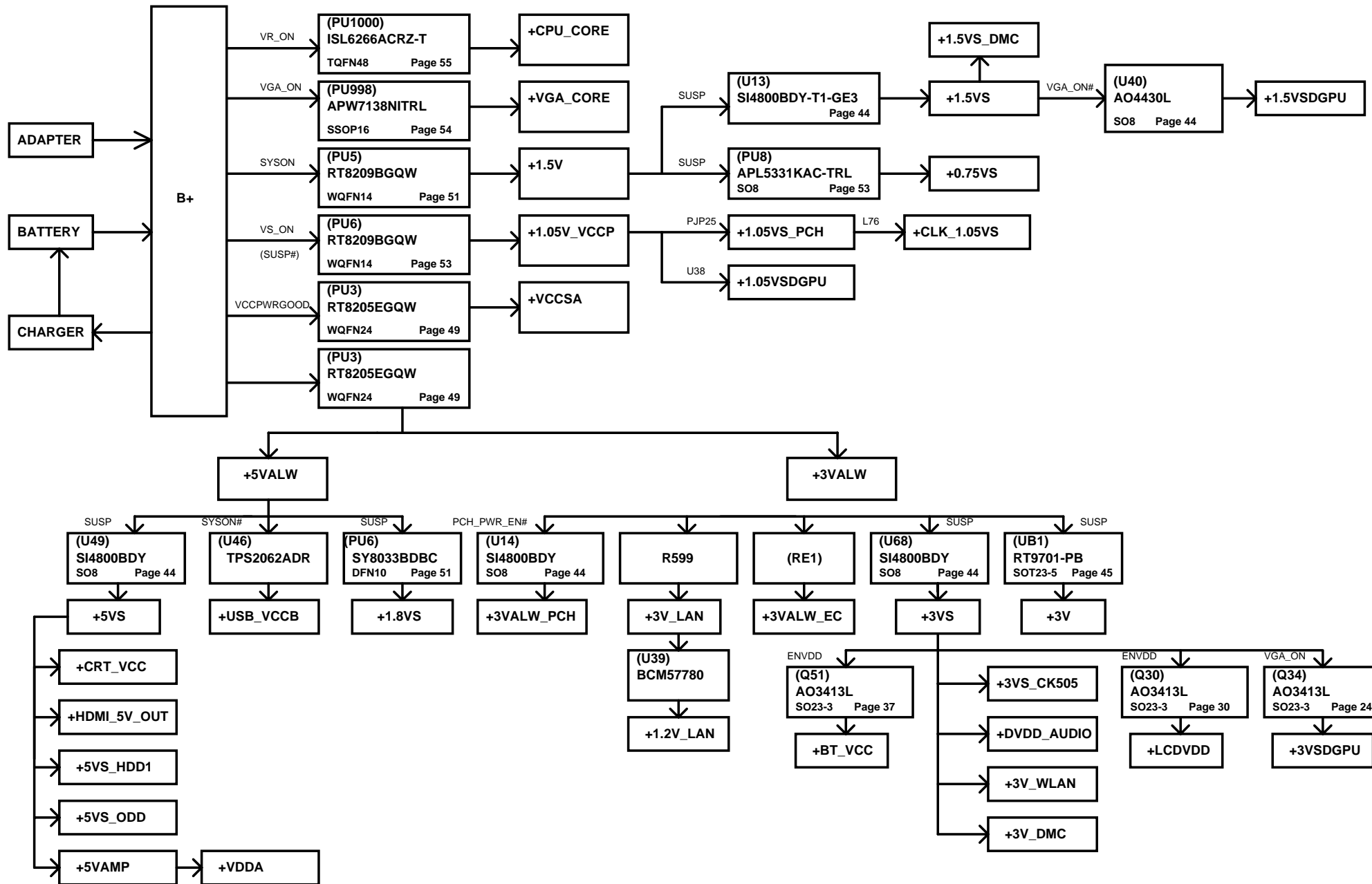
## Version change list (P.I.R. List)

Page 1 of 1  
for PWR

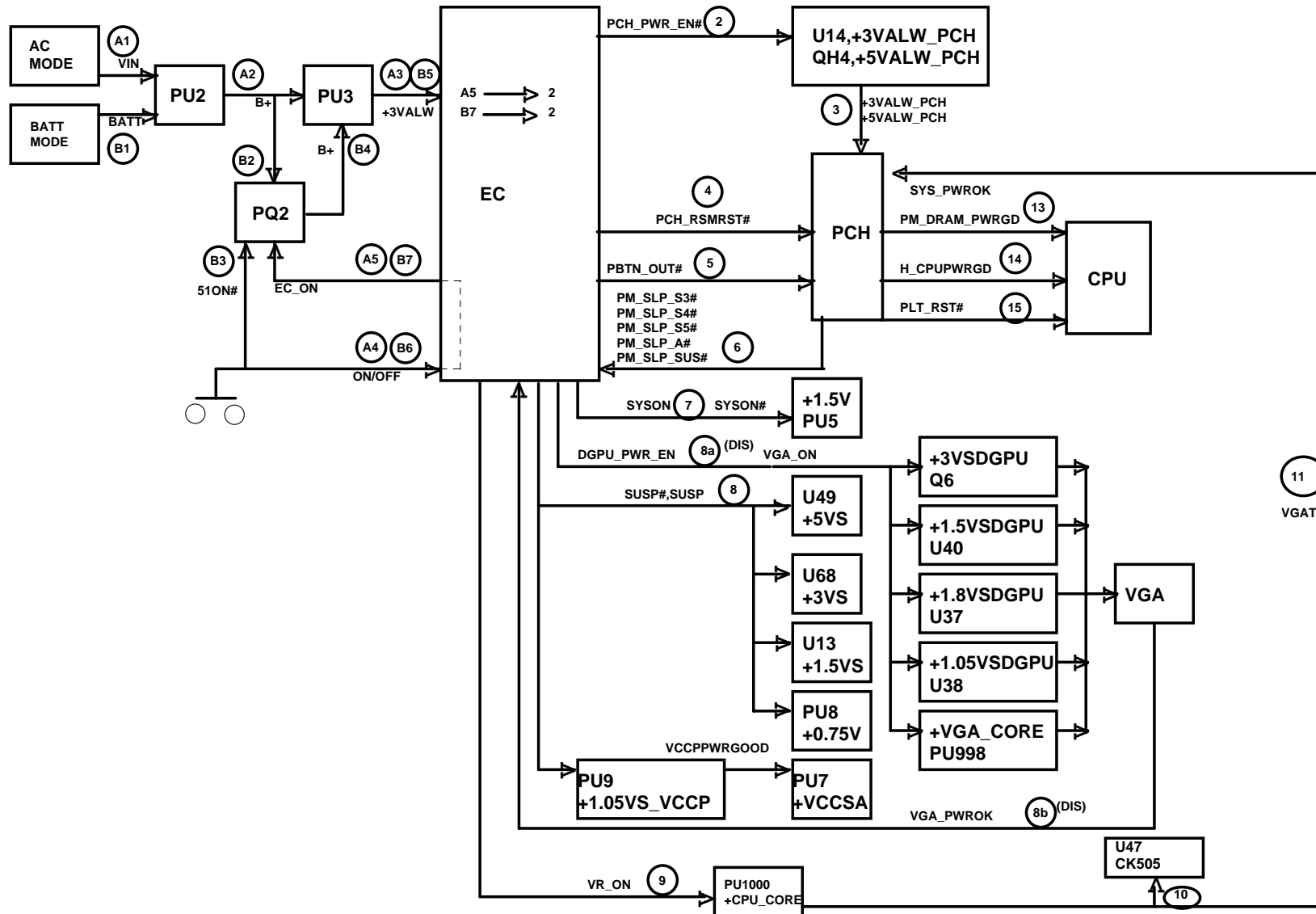
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Add snubber R=4.7 ohm and C 680 pF	EMI solution	0.2	---	Add SD001470B80 for PR35,PR58,PR60,PR87,PR111,PR133,PR202,PR216,PR234 Add SE074681K80 for PC27,PC44,PC45,PC63,PC85,PC100,PC140,PC154,PC169	2010/10/20	DVT_P5WE0
2	Change boost R from 0 to 2.2 ohm	EMI solution	0.2	---	Change R to SD013220B80 for PR37,PR56,PR57,PR85,PR109,PR132,PR186,PR214,PR233	2010/10/20	DVT_P5WE0
3	Change PL11 and PL12 from SH00000F800 to SH00000M700	Cost saving	0.2	52	Change PL11 and PL12 from SH00000F800 to SH00000M700	2010/10/20	DVT_P5WE0
4	Change PL18,PL19,PL20,PL21 from SH000005680 to SH00000HK00	Change DCR tolerance to 5%	0.2	55	Change PL18,PL19,PL20,PL21 from SH000005680 to SH00000HK00	2010/10/20	DVT_P5WE0
5	CPU CORE transient compensation	CPU CORE transient compensation	0.2	55	Add PR248, PC160, PC180	2010/10/20	DVT_P5WE0
6	Fixed adapter plug in will cause could not transition to AC mode when system was on battery mode	disable pre-charge circuit and don't use 運動線路	0.5	---	Del PR7, PR8, PR9, PR10, PR11, PR12, PR13, PD3, PD4, PQ2, PQ3, PQ4, PR18, PR21, PQ12, PC17	2010/11/20	PVT_P5WE0
7	Fixed adapter plug in will cause could not transition to AC mode when system was on battery mode	disable pre-charge circuit and don't use 運動線路	0.5	---	Add PR262, PD10, PQ70, PR263, PC16 Change PQ7 to A04459	2010/11/20	PVT_P5WE0
8	Add 0.1UF on B+ input power	EMI solution	0.5	---	Add PC184, PC185, PC186, PC187	2010/11/20	PVT_P5WE0
9	Adjust VGA CORE power sequesce	for NV request	0.5	---	Change PR149 to 100K	2010/11/20	PVT_P5WE0
10	Adjust 1.5VSDGPU power sequesce	for NV request	0.5	---	Change PR94 to 510K and add PC69	2010/11/20	PVT_P5WE0
11	Adjust VID table	for NV request	0.5	---	Change PR153, PR157, PR160	2010/11/20	PVT_P5WE0
12							
13							
14							
15							

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				PIR (PWR)
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.18	PCH_GPIO71	09/01	SW	For identofy VRAM 900 or 800 MHz		0.2
2	P.31	DPST buffer	09/03	HW	Change U1 from NOT gate to Buffer		0.2
3	P.39	EC_MUTE# pull high	09/03	HW	Change EC_MUTE# Pull high from +3VALW to +3VS		0.2
4	P.40	TP Conn. Reverse	09/03	HW	TP Mudule change,so reverse TP pin		0.2
5	P.13	R624 pop @	09/03	HW	Already pull high R655~		0.2
6	P.45	Change Cap from 0.1u to 0.01u	09/03	HW	C696,C368,C717,C718,C695,C366,C697, C401,C370,C369,C715 change to 0.01U Follow Vendor Suggest ..		0.2
7	P.35	Change 0 Ohm to 47 Ohm	09/04	Broadcom	R199,R207,R211,R215,R168,R171,R179, R182,R195,R216,R192 change to 47 Ohm Follow Vendor Suggest ..		0.2
8	P.5		09/17	HW	CPU XDP socket take off		0.2
9	P.40		09/17	HW	TP pin reverse		0.2
10	P.13		09/17	HW	R624 change to 4.7K		0.2
11	P.45		09/17	HW	OCI2B(R313) place @ for BOM		0.2
12	P.33		09/17	HW	HDMI output from PCH (by UMA)		0.2
13	P.35		09/17	HW	switch the LAN MIDI0 and MIDI2 pin		0.2
14	P.17,35 ,37,38, 39,45		09/17	HW	Change IO port PLT_RST# to PLT_RST_BUF#		0.2
15	P.18		09/17	HW	OPTIMUS_EN# pull high, pull low resistor value both change to 10K		0.2
16	P.24		09/20	HW	modify the VRAM strap pin ROM_SI pull low resistor for implement VRAM 900MHz		0.3
17	P.33		09/23	HW	Add R784 and R785 for DDC pull high...		0.3
18	P.44		09/23	HW	Add C818 and C819 for coupling noise from other spare trace...		0.3
19	P.45		09/23	HW	Add R786,R787,R788 and R789 pull down from vendor's suggestion..		0.3
20	P.37		09/23	HW	Add C820,R790 and Q58 for 3G/B and change source voltage from +3VS to +3VALW..		0.3
21	P.45		09/23	HW	Add C821,C822,C823,C824 for +1.5V... and move the PJ26 & PJ27 between 1.5V to 1.5VSDGPUH		0.3
22	P.46		09/24	HW	Change JUSB5 to USB2.0 Conn. Add D34 as ESD Diode for USB3.0		0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	P.41		09/24	HW	Add R791 pull down 22k Ohm to ground Vendor's request...		0.3
24	P.22		09/24	HW	Add D31 to connect to ACIN Vendor's request...		0.3
25	P.36		09/29	HW	Add JP1,JP2 and JP3 for 家電下鄉 ESD protection		0.3
26	P.36		09/29	ME	Update the JREAD1 symbol		0.3
27	P.13		09/29	HW	Add R792 follow DG1.5		0.3
28	P.33		09/29	HW	Change HDMI termination R to 680 Ohm		0.3
29	P.44		09/29	HW	Add C825 fro +1.05VSDGPU		0.3
30	P.17,38,45		09/30	HW	Change the M/B to USB port to port 1 Sub/B to port 0 and port 2		0.3
31	P.5		10/04	HW	Add test point for TCK,TMS, TRST#,TDO,TDI		0.3
32	P.17,18		10/04	HW	WWAN_OFF# from GPIO51 to GPIO37 WL_OFF# from GPIO55 to GPIO49		0.3
33	P.17,45		10/04	HW	M/B USB port from port 2 change to port1		0.3
34	P.26		10/04	HW	C1 and C604 chaneg to 470uF		0.3
35	P.36		10/04	HW	Add C827 as DGND and RJ45_GND bridge		0.3
36	P.36		10/04	HW	Change R490,R491,R492 and R493 to 0603 package		0.3
37	P.35		10/04	HW	Chaneg R214 to 0603 package		0.3
38	P.35		10/04	HW	Chaneg R192,R195,R199,R207,R211, R215,R168,R171,R179,R182 to 0 Ohm		0.3
39	P.40		10/04	HW	follow broadcom suggestion,add R496		0.3
40	P.40		10/04	HW	Add keyboard cap for EMI		0.3
41	P.44		10/04	HW	Add C826 for +1.5VSDGPU		0.3
42	P.37		10/05	HW	Add RTS5138 circuit		0.4
43	P.13		10/12	HW	Add D35 ,R799 and C838 for changing the RTC to samll size... and can be charged!!		0.4
44	P.14		10/12	HW	Add CLK_SD_48M for Card Reader 5138		0.4
45	P.24		10/12	HW	Pop R129 follow NV suggestion		0.4
46	P.25		10/12	HW	Pop R82 and De-pop R92 follow NV suggestion		0.4
47	P.25		10/12	HW	Add R800 and R801 10K Ohm pull down follow NV suggestion		0.4
48	P.24		10/12	HW	Change R775,R777,R778 and R779 to GV@		0.4

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